UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 130/230A Prof. Liu
Fall 2013

Homework Assignment #11
Due at the beginning of class on Thursday, 11/14/13

Problem 1: Long-Channel MOSFET *I-V* Characteristics

Consider the n-channel Si MOSFET of Homework Assignment #10 Problem 3, with n+ poly-Si gate (Φ_M = 4.05 eV), equivalent oxide thickness T_{oxe} = 3 nm, body dopant concentration $N_A = 5\times10^{17}$ cm^{-3}, channel width W = 5 μm and channel length L = 0.5 μm.

(a) Calculate the bulk charge factor, m.

(b) Sketch the I_{DS} *vs.* V_{DS} curves for V_{GS} = 0.5 V and V_{GS} = 1.0 V, for 0 V ≤ V_{DS} ≤ 1.0 V. Assume that the channel-length modulation parameter λ = 0.1, and that the current in the saturation region of operation is given by the following equation:

$$I_{Dsat} = I_{Dsat0}\left[1 + \lambda\left(V_{DS} - V_{Dsat}\right)\right]$$

Indicate numerical values for V_{Dsat} and I_{Dsat0}.

(c) Indicate **qualitatively** how the I_{DS} *vs.* V_{DS} characteristic for V_{GS} = 1.0 V in part (b) would change if the equivalent oxide thickness were to be decreased, *e.g.* to 2 nm. (Be careful to consider the impact on V_T, μ_{eff}, and m. You may assume that λ does not change significantly with T_{oxe}.)

Problem 2: MOSFET Small-Signal Model

A MOSFET can be used to amplify a small analog voltage signal applied to its gate electrode, by connecting a resistor to its drain to generate an analog output voltage signal across this "load". Typically, a DC gate voltage is applied to the MOSFET to "bias" it in the saturation region of operation. The transconductance g_m (defined as the change in drain current induced by a change in gate voltage) of the transistor is an important parameter for amplifier applications; a larger value of g_m is desirable for higher amplifier gain.

(a) What is the value of g_m for the MOSFET of Problem 1, for a gate voltage of 1 V? You may neglect the impact of channel length modulation (λ) for this calculation.

(b) Indicate how the transconductance of an n-channel MOSFET can be improved by changing the following design parameters. (Would you want to increase or decrease the following parameters to increase g_m?)

- **(i)** Equivalent gate oxide thickness (T_{oxe})
- **(ii)** Body dopant concentration (N_A)
- **(iii)** Channel length (L)

Problem 3: MOSFET Sub-Threshold Current

In a complementary metal-oxide-semiconductor (CMOS) digital logic circuit, power is consumed in steady state (when neither the input voltages nor the output voltage are changing with time) due to transistor off-state leakage current I_{OFF}, *i.e.* the current which flows when $|V_{GS}| = 0$V and $|V_{DS}|$ is greater than zero. To reduce this "standby" power consumption, low I_{OFF} is desirable. At the same time, high transistor on-state current I_{ON} is desirable for fast digital circuit operation, since the time required to change the output voltage (*i.e.* propagation delay) is directly proportional to I_{ON}.

For a MOSFET operating in the subthreshold regime ($V_{GS} < V_T$), the reduction in gate voltage needed to reduce the drain current by one decade (*i.e.* a factor of 10) is defined as the "subthreshold swing" S:

$$\boldsymbol{S = (kT/q)(ln\ 10)[1 + (C_{dep}/C_{ox})] = (kT/q)(ln\ 10)[m]}$$

The units of S are mV/decade. Note that the smallest value of S attainable at room temperature (300K) is 60 mV/decade. **Consider the MOSFET of Problem 1, but suppose the threshold voltage for this device is defined to be the value of V_{GS} at which the normalized drain current $I_{DS}/(W/L)$ reaches 100 nA, for V_{DS} = 100 mV.**

(a) If the leakage current must be less than or equal to 1 pA when V_{GS} = 0 V and V_{DS} = 100 mV, what is the minimum threshold voltage this device can have?

(b) Qualitatively, how would your answer to part (b) change if the leakage current specification were to be relaxed, *e.g.* to 100 pA? What would be the implication for transistor drive current (*i.e.* I_{Dsat})?

(c) Why is a small value of S desirable? (Hint: Consider the trade-off between low I_{OFF} and high I_{ON}, with respect to the threshold voltage V_T.)

Problem 4: MOSFET Design Project Preparation

This exercise is intended to help you prepare to run MOSFET simulations using the software package Synopsys Sentaurus, in preparation for your design project. You will need to use your EE class computer account.

(a) If you plan to team with a partner for the MOSFET design project, please indicate his/her name.

(b) After watching the video tutorial on using Sentaurus (to be posted on the course website soon), download and unpack the project within Sentaurus workbench. (This simulation setup will be used for your course project.) Afterwards, familiarize yourself with the basic simulation frames.
Briefly describe the purpose of each simulation component:
(i) Sentaurus Structure Editor (SDE)
(ii) Sentaurus Device (SDEVICE)
(iii) Sentaurus Inspect (INSPECT)

(c) Preprocess the whole simulation flow. In the SDE simulation, find and run the node which gives you the generated device structure. Use SVisual (Sentaurus Visual) to generate the device structure and print it out. Turn it in with your assignment.

(d) Extract and plot the absolute doping concentration as a function of distance along the channel direction (from the source region to the drain region), at a distance 2 nm beneath the SiO_2/Si interface.