UNIVERSITY OF CALIFORNIA
College of Engineering
Department of Electrical Engineering and Computer Sciences

EE 130 / EE 230A — Prof. Liu
Fall 2013

Homework Assignment #5
Due at the beginning of class on Thursday 10/3/13

Problem 1: Schottky diode *I-V* characteristics

A Schottky diode maintained at $T = 300$ K is formed between NiSi (which is employed in the most advanced CMOS technologies today) and silicon doped with 10^{16} cm^{-3} phosphorus. The cross-sectional area is 100 μm × 100 μm = 10^{-4} cm^2.

(a) Determine the reverse saturation current I_S, using the measured value of Schottky barrier height given in Lecture 7 (Slide 8). Recall from Lecture 4 that the conductivity effective masses for electrons and holes in silicon are $0.26m_0$ and $0.39m_0$ (where $m_0 = 9.1\times10^{-31}$ kg) respectively.

(b) **Plot *I vs.* V_A on a semi-log plot (*i.e.* *I* on a log scale and V_A on a linear scale),** for V_A in the range from 0.05 V to 0.4 V. At what value of V_A does $I = 1$ mA? (This is a typical level of current.)

Problem 2: Practical ohmic contact

Consider a MS junction formed by NiSi in contact with uniformly doped silicon, maintained at $T = 300$K. This junction can pass significant current with a small bias ($V_A \neq 0$ V) by quantum-mechanical tunneling of majority carriers into the silicon, if the barrier seen by the carriers is sufficiently narrow, *i.e.* if the junction depletion width W is less than 10 nm.

(a) What is the minimum value of N_D such that this condition is met for a NiSi contact to n-type Si? (From Lecture 7 Slide 8, the Schottky barrier height for electrons, Φ_{Bn}, is 0.65 eV.) You may assume that $qV_{bi} \cong \Phi_{Bn}$, as shown in Lecture 8 Slide 7.

(b) What is the minimum value of N_A such that this condition is met for a NiSi contact to p-type Si? (From Lecture 7 Slide 8 the Schottky barrier height for holes, Φ_{Bp}, is 0.47 eV.) You may assume that $qV_{bi} \cong \Phi_{Bp}$.

(c) Considering your answers to (a) and (b), is it easier to form a practical ohmic contact to p-type or n-type silicon? Why?

Problem 3: Contact resistance

(a) Typically, the specific contact resistivity, ρ_c, for a silicide contact to heavily doped silicon is **~10^{-8} Ω-cm^2**. In the most advanced CMOS technologies today, the area (A_c) of a silicide contact to the heavily doped source and drain regions of a MOSFET can be as small as $3F^2$, where F is the minimum half-pitch. Calculate the contact resistance $R_c = \rho_c/A_c$ of such a minimum-sized contact, for $F = 22$ nm (relevant to Intel's most advanced CMOS technology). Is the contact resistance significant compared to the intrinsic Si MOSFET on-state resistance which is ~10 kΩ?

(b) Compound semiconductor materials such as GaAs eventually may be used in n-channel field-effect transistors for digital logic applications, due to their higher electron mobility (corresponding to a lower conductivity effective mass) as compared against Si. A practical technological challenge is achieving low source/drain-contact resistance to n-type GaAs, however. Considering that the electron affinity of GaAs is similar to that of Si, and that the solid solubility of n-type dopants (donors) is ~100× lower than in Si, explain why this is the case.

Problem 4: pn junction electrostatics

Consider a silicon step junction maintained at $T = 300$K under equilibrium conditions (*i.e.* with zero applied voltage) with p-side doping $N_A = 1\times10^{16}$ cm^{-3} and n-side doping $N_D = 1\times10^{17}$ cm^{-3}.

a) Calculate the built-in voltage, V_{bi}.

b) Calculate the depletion region width, W. What are x_p and x_n?

Note that $x_p = \dfrac{N_D}{N_A + N_D} W$ and $x_n = \dfrac{N_A}{N_A + N_D} W$

c) What is the electrostatic potential at $x = 0$ (*i.e.* how much voltage is dropped across the p-side)?

Note that $V(0) = \dfrac{qN_A}{2\varepsilon_s} x_p^2 = V_{bi} - \dfrac{qN_D}{2\varepsilon_s} x_n^2$

d) Calculate the peak electric field (at $x = 0$): $\mathcal{E}(0) = \dfrac{2V_{bi}}{W}$

e) Using the values obtained in (a)-(d), sketch the charge density distribution $\rho(x)$, electric field distribution $\mathcal{E}(x)$, and electrostatic potential $V(x)$.

f) Show qualitatively (on your sketches from (e)) how an applied forward bias ($V_A > 0$ V) affects the depletion region width W, the voltage dropped across the depletion region, and the peak electric field $\mathcal{E}(0)$.