PROBLEM SET #11

Issued: Tuesday, Nov. 19th, 2013

Due: Wednesday, Nov. 27th, 2013, 8:00 a.m. in the EE 140/240A homework box

1. Cancelling a pole with a zero in a two stage op-amp might prove beneficial for stability from a phase margin standpoint. However, if the zero does not land exactly on top of the pole, a doublet is possible that can actually degrade stability. Suppose the open-loop transfer function of a two-stage amplifier is expressed as:

$$H_{open}(s) = A_0 \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$

Ideally $\omega_z = \omega_{p2}$ and the feedback circuit exhibits a first-order behavior, i.e., its step response contains a single time constant and no overshoot.

a. Find the transfer function of the amplifier in a unity gain feedback loop.

b. Determine the two poles of the closed-loop transfer function, assuming they are widely spaced.

c. Determine the small-signal step response of the closed-loop amplifier.

d. Show that the step response contains an exponential term of the form $\left(1 - \frac{\omega_z}{\omega_{p2}}\right) e^{-\omega_{p2} t}$.

2. The amplifier *a(s)* has one negative real pole and is configured as an inverting feedback amplifier as shown in Fig. PS11.2.

a. Calculate the DC gain of the amplifier *a(s)* such that the static gain error of the feedback amplifier is 0.05%.

b. Calculate the pole location such that the settling time is 10ns for 0.05% accuracy.

c. If the open loop amplifier has a second pole that produces 60% phase margin for the feedback configuration in Fig. PS11.2, what is the new settling time? For this part you can use either analytical methods or numerical simulations.

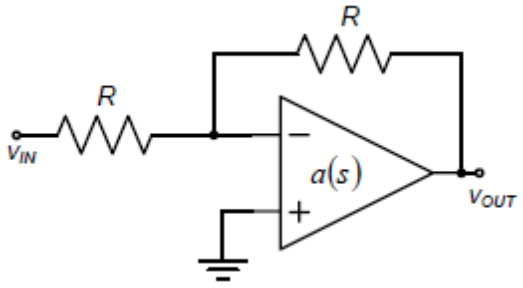
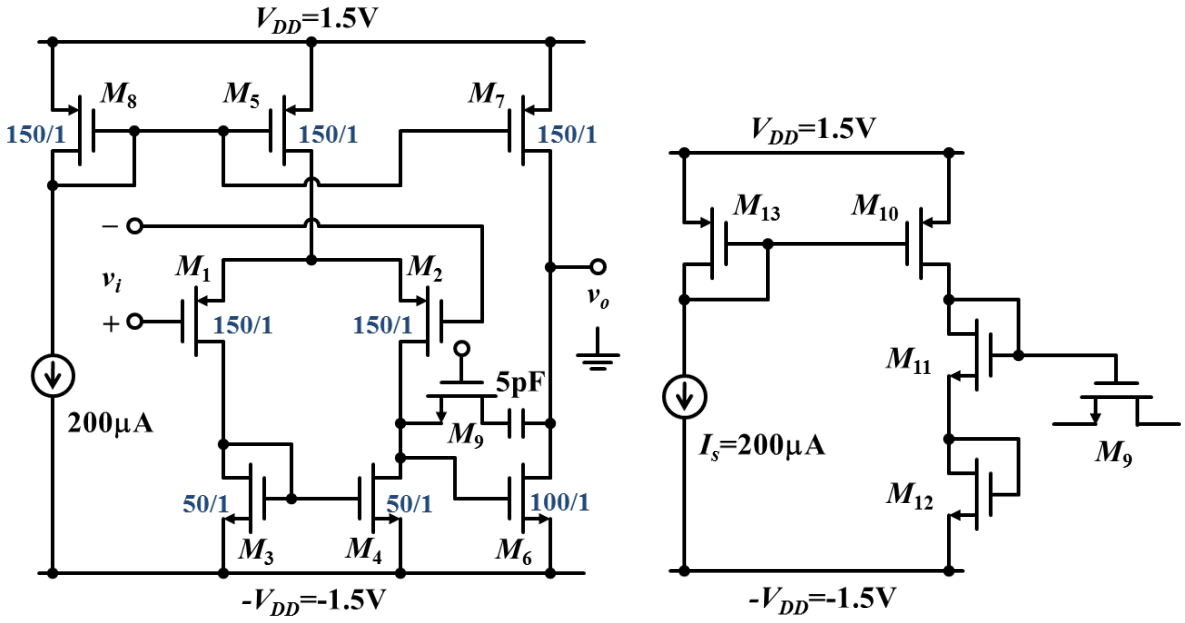


Fig. PS11.2

3. This problem concerns the CMOS op-amp shown in Fig. PS11.3.



(a) **(b)**

Fig. PS11.3

Variable	NMOS	PMOS	Unit
X_d	0.1	0.1	μm
dX_d/dV_{ds}	0.02	0.04	μm/V
t_{ox}	80	80	A
μ	450	150	cm^2/Vs
V_t	0.7	0.7	V
γ	0	0	$V^{-1/2}$

Table PS11.3

a. Calculate the open-loop voltage gain, unity-gain bandwidth, and slew rate, for the circuit in Fig. PS11.3 (a). Use the parameters of Table PS11.3. Assume that the gate of M_9 is connected to the positive power supply V_{DD} and that the W/L ratio of M_9 has been chosen to cancel the right half-plane zero.

b. If the circuit of Fig. PS11.3 (b) is used to generate the voltage to be applied to the gate of M_9 in Fig. PS11.3 (a), calculate the required W/L ratio of M_9 to move the right-half plane zero to infinity. Let V_{DD} = 1.5V and I_s = 200μA. Use L = 1μm for all transistors, W_{13} = W_{10} = 150μm, and W_{11} = W_{12} = 100μm. Use Table PS11.3 for other parameters.

c. Assuming that the zero has been moved to infinity, determine the maximum load capacitance that can be attached directly to the output node of the circuit in Fig PS11.3 (a) and still maintain a phase margin of 45°. Neglect all higher order poles except the one due to the load capacitance. Use the value of W/L ratio obtained in part (b) for M_9 with the bias circuit of Fig. PS11.3 (b). Ignore junction capacitance for all transistors. Use Table PS11.3 for other parameters.

4. In this problem, you will simulate using Hspice the op amp given in "ee140_hw11.sp." Its accompanying device model is given in "ee140_hw11_model.sp." For your convenience, the op amp circuit is pictorially shown below in Fig. PS11.4. Please give all gain values and ratios in dB.

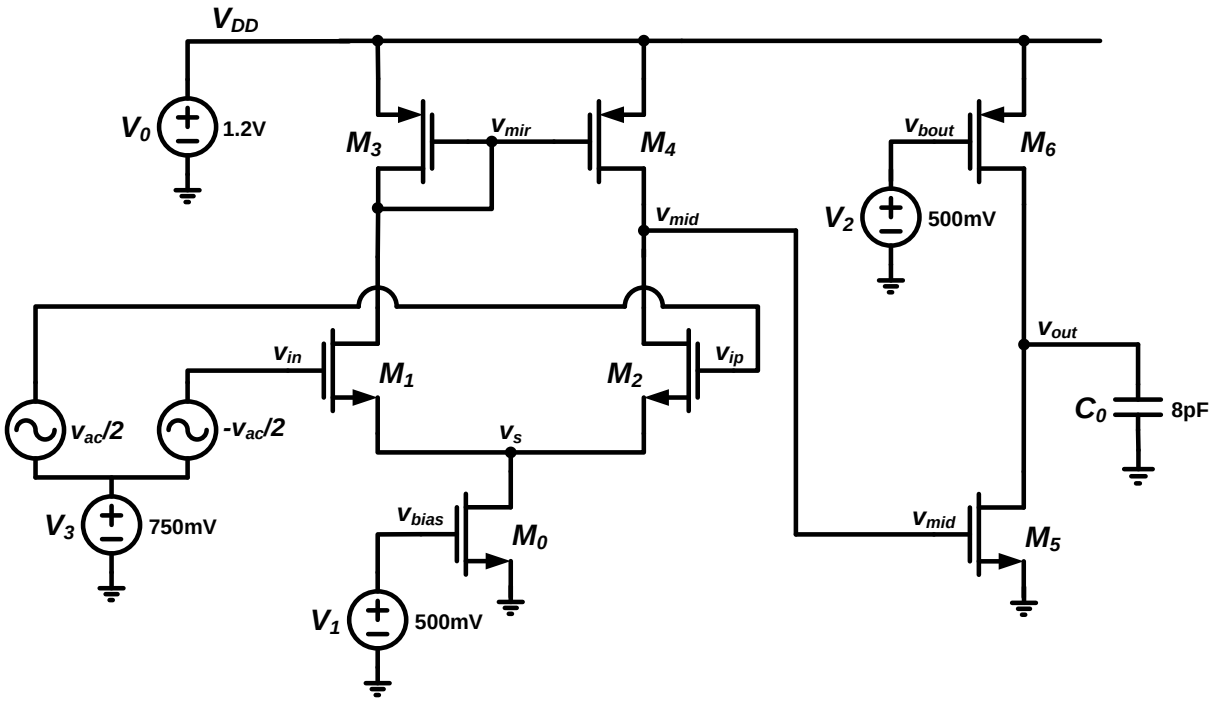


Fig. PS11.4

a. Simulate the open loop AC gain and phase of the op amp. What is the op amp's gain at low frequencies? What is the op amp's unity gain frequency? What is the op amp's unity gain phase margin?

b. Simulate the common mode gain of the op amp by applying positive v_{ac} to both inputs. What is the op amp's common mode gain at low frequencies? What is the op amp's CMRR?

c. Simulate the power supply gain of the op amp:

i. Turn off the AC signal at the op amp's inputs.

ii. Add an AC signal to the power supply voltage source *V0*.

What is the op amp's power supply gain at low frequencies? What is the op amp's PSRR?

d. Simulate the output swing of the op amp using DC sweep analysis:

i. Sweep the DC voltage at one of the op amp's inputs around its bias point.

ii. Take the derivative of the op amp's DC output voltage with respect to the swept input. Make sure there is enough resolution in your sweep to get an accurate result.

For the purpose of this course (and your project), we will define the op amp's output swing range as the DC output voltages at which dV_{out}/dV_{in} becomes 1/10 the nominal differential gain (from part (a)). What is the op amp's output swing range?

e. Simulate the common mode input range of the op amp using DC sweep analysis:

i. Put the op amp into unity gain feedback.
ii. Sweep the DC voltage of the op amp's input from 0 to VDD.
iii. Take the derivative of the op amp's DC output voltage with respect to the swept input.

For the purpose of this course (and your project), we will define the op amp's input range as the DC input voltages at which dV_{out}/dV_{in} becomes 1/2 in unity gain feedback. What is the op amp's common mode input range?