

PROBLEM SET #3

Issued: Tuesday, Sep. 17th, 2013

Due: Wednesday, Sep. 25th, 2013, 8:00 a.m. in the EE 140/240A homework box

1. Referring to the multistage amplifier circuit shown in Fig. PS3.1:

- Calculate the DC operating points including the current flowing through each branch and DC voltage at each node.
- Calculate transistor small-signal parameters (i.e. g_m , r_π , r_o , C_π , C_μ , C_{gs} , C_{gd}).
- Provide expressions and calculate the numerical values for the input resistance, R_{in} ; output resistance, R_{out} ; first stage gain, v_{o1}/v_s ; second stage gain, v_{o2}/v_{o1} ; third stage gain, v_{out}/v_{o2} and total gain, v_{out}/v_s .
- Estimate the low frequency cut-off f_L and high frequency cut-off f_H of the amplifier.

BJT parameters:

$$\beta = 100, V_A = 50V, V_{BE(on)} = 0.7V, V_{CE(SAT)} = 0.2V, \tau_F = 150ps, C_{je} = 50fF, C_\mu = 0.1pF, V_T = 25mV, C_{cs} = 50fF.$$

MOS parameters:

$$V_{th0} = 0.5V, k' = 160\mu A/V^2, W/L = 8\mu m/1\mu m, C_{ox} = 30\mu F/cm^2, C_{ot} = C_{db} = C_{sb} = 0.1pF, \lambda = 0.05V^{-1}, \gamma = 0.$$

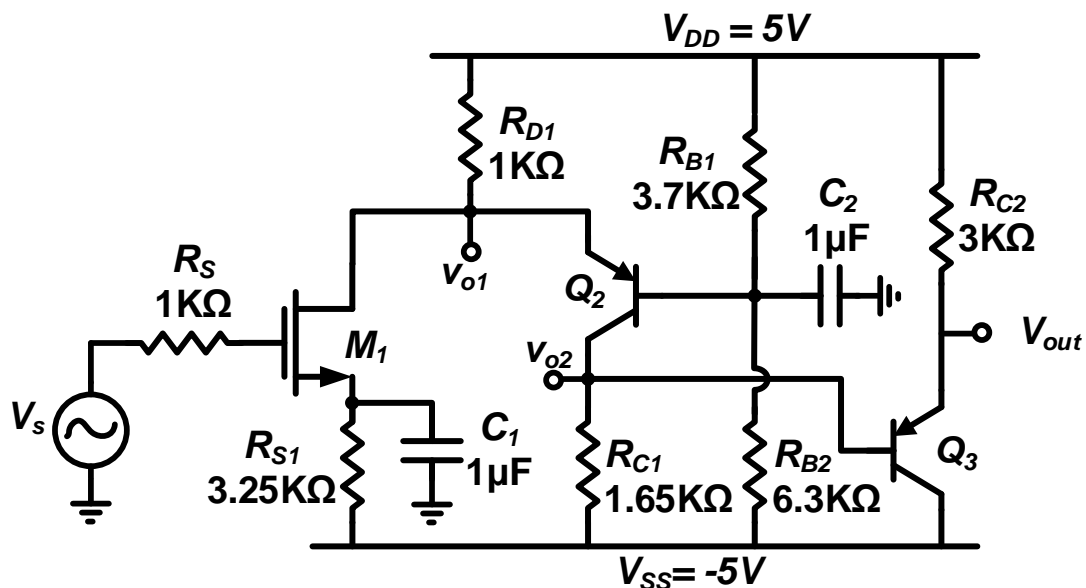


Fig. PS3.1

2. For the small-signal circuits shown in Fig. PS3.2, assume all transistors are identical and have the following parameters:

$$I_D = 2\text{mA}, W = 50\mu\text{m}, L_{\text{drawn}} = 130\text{nm}, L_d = 15\text{nm}, X_d = 0, k' = 200\mu\text{A}/\text{V}^2, \gamma = 0, \lambda = 0, C_{ox} = 15\text{fF}/\mu\text{m}^2, C_{sb} = C_{db} = 0.$$

Given $R_S = 500\Omega$, $R_L = 1\text{k}\Omega$, and $C_L = 50\text{fF}$:

- (a) Calculate the mid-band, small-signal voltage gain v_o/v_i for each circuit.
 (b) Calculate and compare the high 3-dB cutoff frequencies of the two circuits.

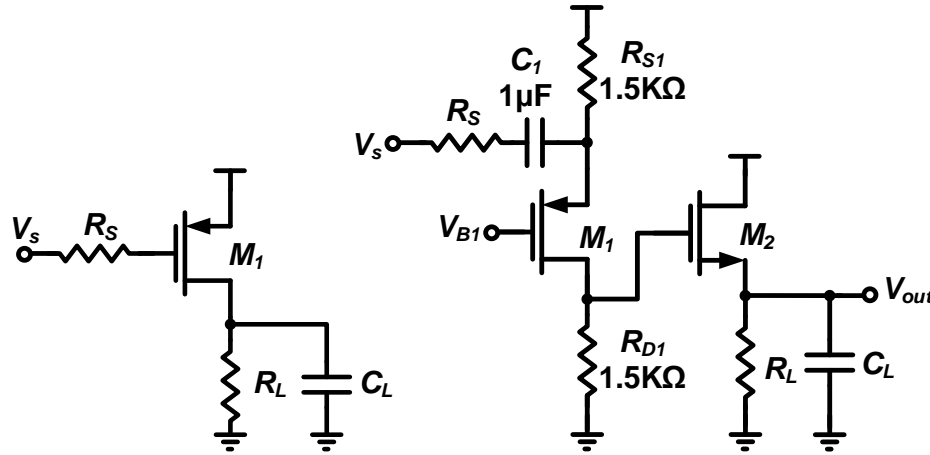


Fig. PS3.2

3. This problem investigates single-stage amplifier design.

Use the following parameters:

$$\mu_n C_{ox} = 100\mu\text{A}/\text{V}^2, \mu_p C_{ox} = 50\mu\text{A}/\text{V}^2, V_t = 0.5\text{V}, V_{DD} = 3\text{V}, L = 1\mu\text{m}, W_p = 2 W_n, (V_{GS} - V_t)_{\text{min}} = 100\text{mV} \text{ for strong inversion}, C_L = 4\text{pF}, C_{gs} = 1\text{pF}, C_{gd} = 0\text{pF}, C_{db} = C_{sb} = 1\text{pF}$$

- a) What is the maximum mid-band voltage gain of a resistively loaded common source amplifier operating in strong inversion? Use $\lambda_n = \lambda_p = 0$.
 b) How about with an active (PMOS) load? $\lambda_n = \lambda_p = 0.1\text{V}^{-1}$.
 c) If $I_D = 1\text{mA}$, how would you size each of the devices for maximum voltage gain?
 d) With $I_D = 1\text{mA}$, what is the dominant pole frequency of each of these amplifiers?

4. Fig. PS3.4 shows a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies. For our purpose here, we shall assume that the capacitors are large enough to act as perfect short circuits at all signal frequencies of interest.
- Find the dc bias current in each of the three transistors. Also find the dc voltage at the output. Assume $|V_{BE}| = 0.7\text{V}$, $\beta = 100$, and neglect the early effect.
 - Find the input and output resistance.
 - Calculate the voltage gain v_o/v_i .

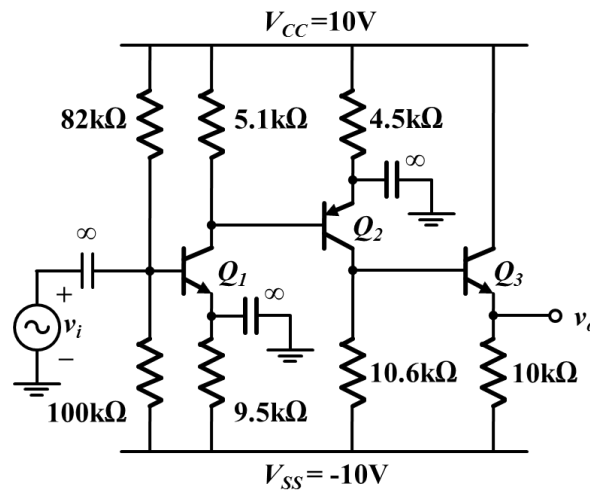


Fig. PS3.4