PROBLEM SET #5

Issued: Tuesday, Oct. 1st, 2013

Due: Wednesday, Oct. 9th, 2013, 8:00 a.m. in the EE 140/240A homework box

1. Calculate the output current I_{OUT} of the CMOS Widlar current source shown in Fig. PS5.1. Here, I_{IN} = 100μA, V_{DD} = 3V, $(W/L)_1=(W/L)_2$ = 25, k' = 200μA/V^2 and R_2 = 4kΩ. Assume λ = 0 and ignore the body effect.

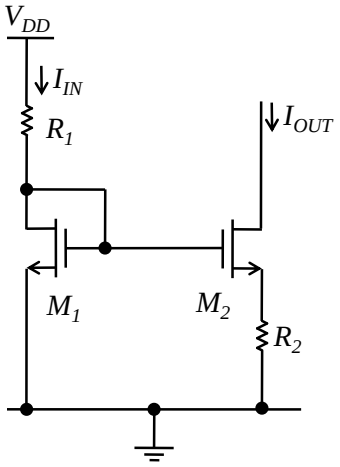

Fig. PS5.1

2. Design the circuit shown in Figure PS5.2 to meet the following constraints:

a) Transistor M_2 operates in the saturated region for values of V_{OUT} to within 0.2V of ground.

b) The output current must be 50μA.

c) The output current must change less than 0.02% for a change in output voltage of 1V.

You are to minimize the total device area within the given constraints. Here the device area will be taken to be the total gate area ($W\times L$ product). Ignore the body effect for simplicity. Make all devices identical except M_4. Use the following process parameters: t_{ox} = 8nm, μ_n = 450cm^2/VS, L_d = 0.09μm, dX_d/dV_{DS} = 0.02μm/V (channel length modulation parameter, use it to get λ).

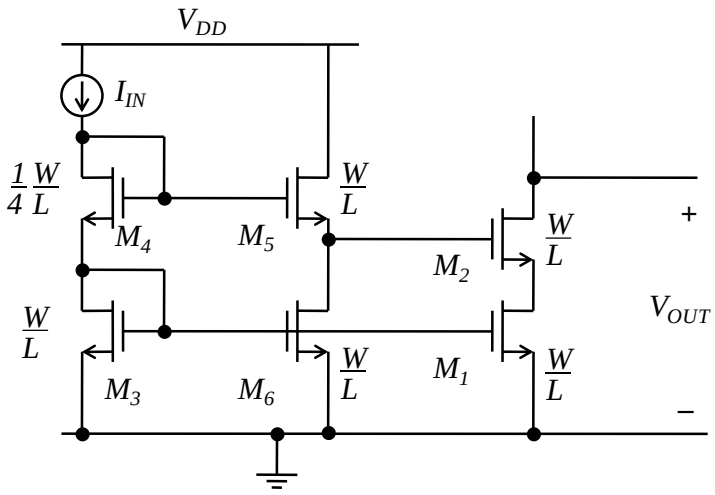

Fig. PS5.2

3. For the current source circuit shown in Fig. PS5.3, assume $V_t = 0.7\text{V}$, $k' = 110\mu\text{A/V}^2$, $\gamma = 0.4$, $\lambda = 0.04\text{V}^{-1}$, $2|\varphi_f| = 0.7$.

a) Design the size of M_4 to allow a minimum output voltage of $2V_{OV,\,M1}$. (You may ignore body effect for this part.)

b) Considering the body effect, what is the minimum output voltage that ensures all transistors are in saturation region? What is the output resistance?

c) Suppose the reference current sources are reduced to 5μA. Size M_3 and M_4 to achieve the same output current as that of the circuit in part (a).

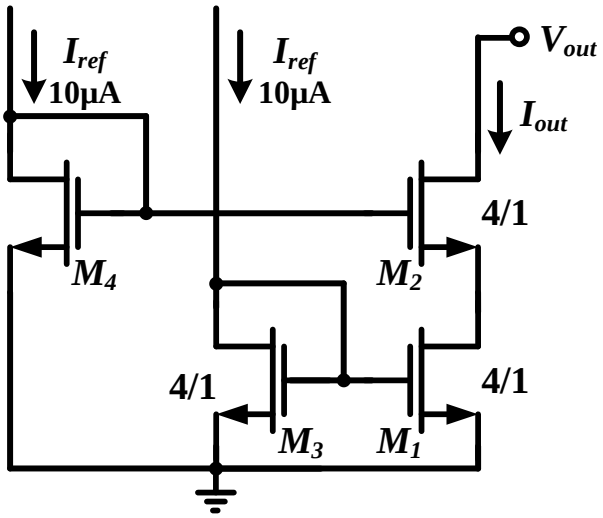

Fig. PS5.3

4. This problem concerns the simple MOS current mirror shown in Figure PS5.4a.

(a) Design the current mirror such that all of the following is satisfied:

i. The currents I_2 = 0.5mA and I_3 = 2mA (approximately).
ii. The minimum output voltage for which M_2 and M_3 work as current sources is 200mV.
iii. The output currents change less than 1% for a change in output voltage of 1V.
iv. All transistors should have the same channel length.

You are to minimize the total circuit area which is approximately given by

$$A = \sum_{i=1}^{3} W_i L_i + \beta R_1$$

The parameter λ can be calculated as $\lambda = \alpha/L$. α and β are constants.

$$\alpha = 0.02\frac{\mu m}{V}, \beta = 0.2\frac{\mu m^2}{\Omega}, C_{ox} = 5\frac{fF}{\mu m^2}, \mu_n = 450\frac{cm^2}{Vs}, V_{th} = 0.6V$$

(b) A layout designer used long and narrow wires to connect sources of M_1, M_2, and M_3, which resulted in small parasitic resistances R_p = 2Ω, as shown in Figure PS5.4b. What are the new values of I_2 and I_3? You can use numerical methods if needed.

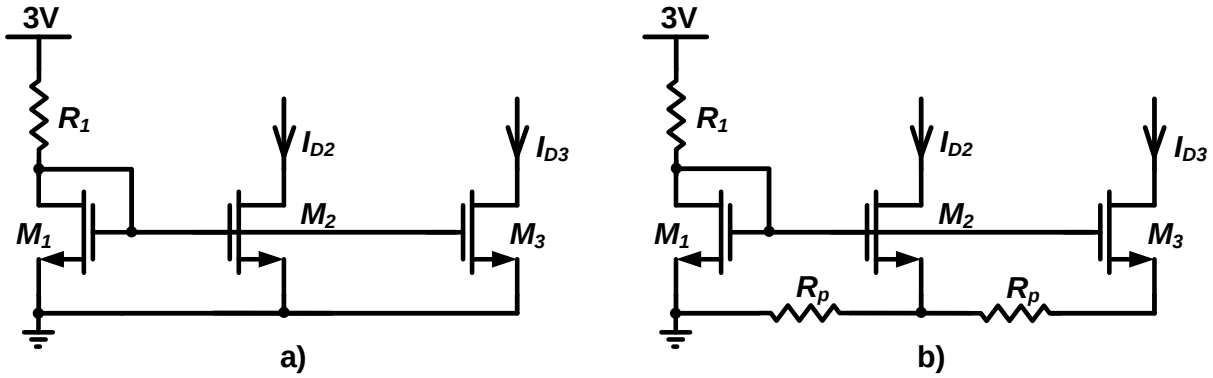

Fig. PS5.4