PROBLEM SET #6

Issued: Tuesday, Oct. 8st, 2013

Due: Wednesday, Oct. 16th, 2013, 8:00 a.m. in the EE 140/240A homework box

1. For the high-swing cascode mirror shown in Fig. PS6.1 answer the following questions:

a) Calculate W such that the minimum output voltage for which both M_1 and M_2 are in saturation is 0.5V. Assume that M_3-M_5 can provide appropriate gate biases for M_1 and M_2.

b) Calculate W_5 in order to achieve the minimum output voltage calculated in (a).

c) Briefly explain the function of M_4.

d) What is the output resistance of this current source?

e) What is the change in I_{OUT} for ΔV_{OUT}=1V?

f) What is the resistance seen by the I_{IN} that biases M_3 and M_4?

g) Calculate input voltages V_{IN1} and V_{IN2}.

h) Replace transistors M_5 and M_6 with one diode connected device. What is the W of the new device?

$$I_{IN}=100\mu A,\quad L=1\mu m\quad C_{ox}=5\frac{fF}{\mu m^2},\quad \mu_n=450\frac{cm^2}{Vs},\quad V_{th0}=0.6V,\quad \lambda=0.02V^{-1},\quad \gamma=0$$

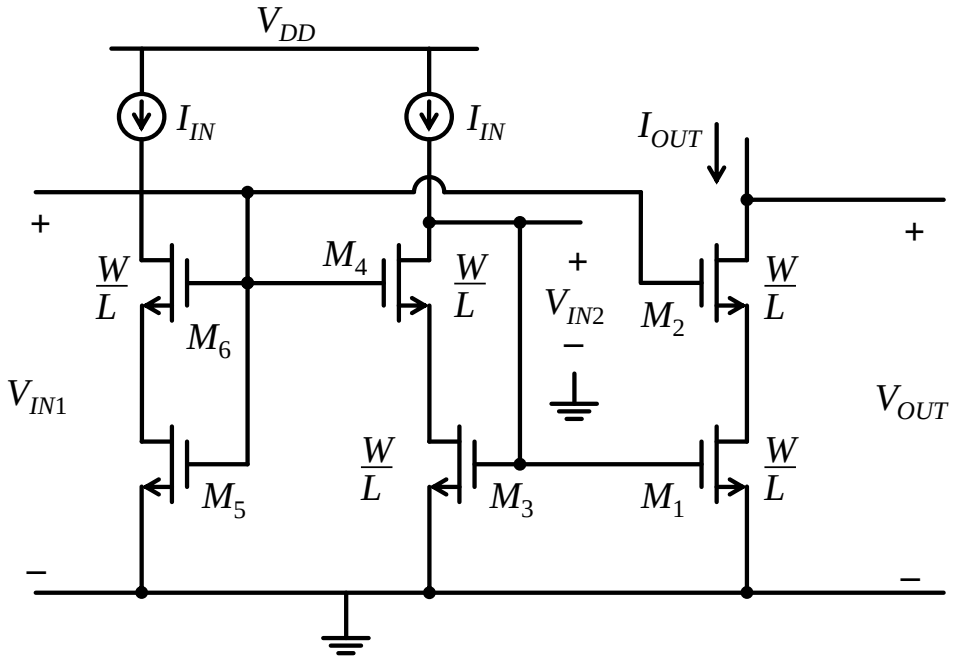

Fig. PS6.1

2. Consider the low voltage cascode current mirror shown in Fig. PS6.2, for which 10μA reference ideal current sources I_1 and I_2 are available, and the desired output current is $I_{OUT} = 100\mu A$. Assuming the size of M_3 is (W/L), determine the (W/L)'s of M_1, M_2, M_4, and M_5 relative to that of M_3 to provide the maximum headroom at the I_{OUT} node. In your design, M_1, M_2, M_3, and M_4 should all have the same V_{ov} and be operating in saturation. Assume $\lambda = 0$ and ignore the body effect.

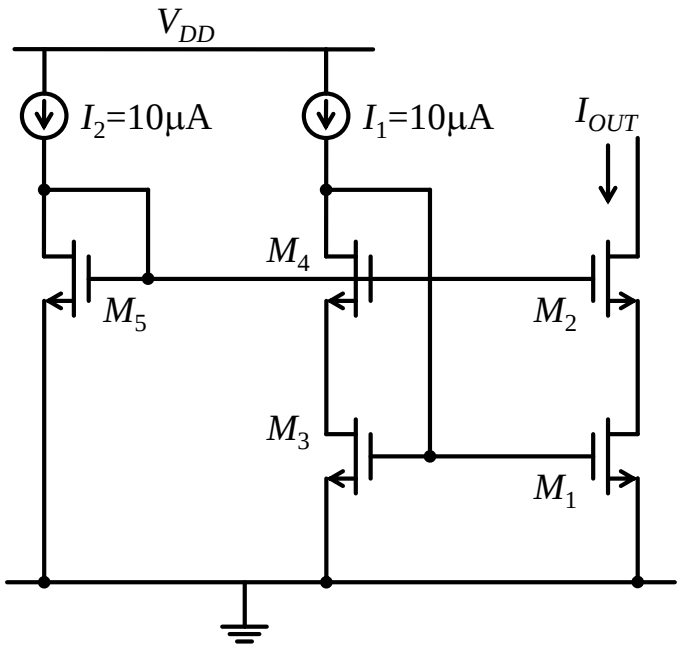

Fig. PS6.2

3. In the circuit shown in Fig. PS6.3, a source follower using a wide transistor M_4 and a small bias current is inserted in series with the gate of M_3 so as to bias M_2 at the edge of saturation. Assuming M_0 - M_3 are identical and $\lambda \neq 0$, estimate the mismatch between I_{out} and I_{REF} if:

(a) $\gamma = 0$

(b) $\gamma \neq 0$

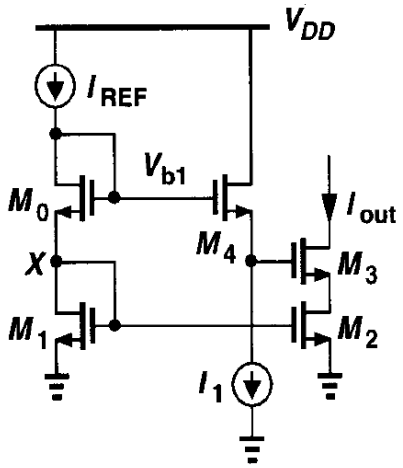

Fig. PS6.3

4. Provide an expression and calculate a numerical value for the output current mismatch between I_{C2} and I_{C3} shown in Fig. PS6.4 caused by finite fabrication tolerances.

Nominal parameter values:

$\beta = 100$, $I_s = 37.751 \times 10^{-15}$A, $V_T = 25$mV, $R_0 = 3.4$kΩ, $R_1 = R_2 = R_3 = 1$kΩ.

Fabrication tolerances:

$\Delta\beta/\beta = 10\%$, $\Delta I_s/I_s = 5\%$, $\Delta R/R = 20\%$.

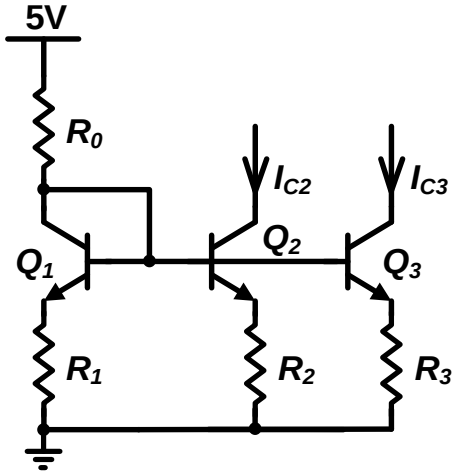

Fig. PS6.4