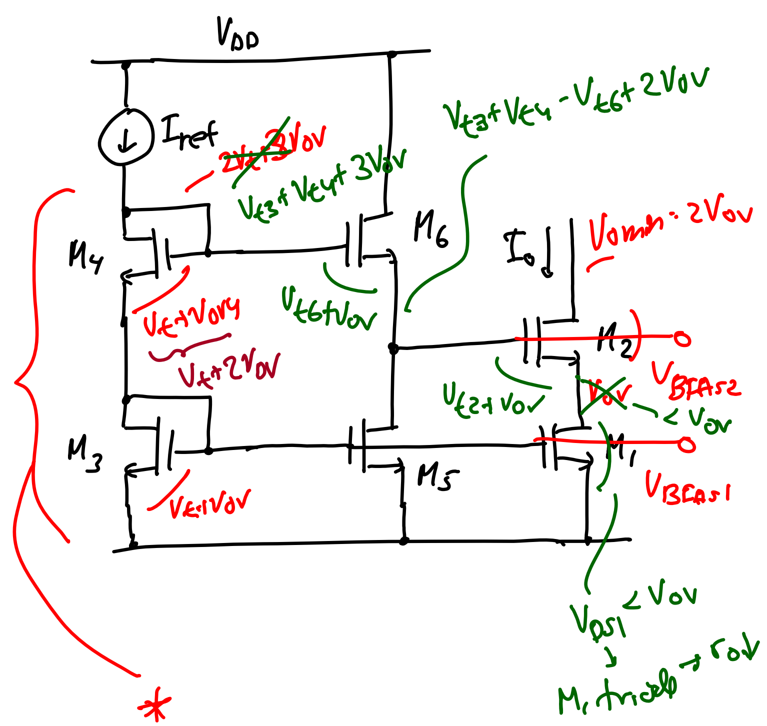
Lecture 12: Current Source Matching

- **Announcements:**
  - Lab#2 online: starts this week
  - HW#6 online soon
  - 240A HW#1A online soon
- **Lecture Topics:**
  - High Swing Current Sources (cont.)
  - Current Source Matching Considerations
  - Op Amp Review
- ------------------------------------
- **Last Time:**

Problem: Body effect $M_4, M_6, M_2 \rightarrow$ increases their V_t's



$V_{t4} \stackrel{?}{=} V_{t6} \rightarrow$ $V_{S4} = V_t + V_{ov}$, $V_{S6} = V_t + 2V_{ov}$ $\Big\}$ $V_{t6} > V_{t4}$,

$$V_t = V_{to} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right) \rightarrow V_{SB}\uparrow \rightarrow V_t\uparrow$$

Problem if this makes $V_{DS1} < V_{ov}$ ($M_1 \rightarrow$ triode)

What is this voltage? (V_{D1}) — very bad!

$V_{t4} + V_{t3} - V_{t6} - V_{t2} + V_{ov}$

$$\underbrace{(V_{t4}-V_{t6})}_{(-)} + \underbrace{(V_{t3}-V_{t2})}_{(-)} + V_{ov} < V_{ov} \rightarrow V_{D1} < V_{ov}$$

M_1 not saturated!

Solutions:

① Remove $\gamma \rightarrow$ tie the wells M_4, M_6, & M_2 to their sources $\rightarrow V_{SB} = 0V$

$$V_t = V_{to} + \gamma\left(\sqrt{2|\phi_F| + \cancel{V_{SB}}} - \sqrt{2|\phi_F|}\right) = V_{to}$$

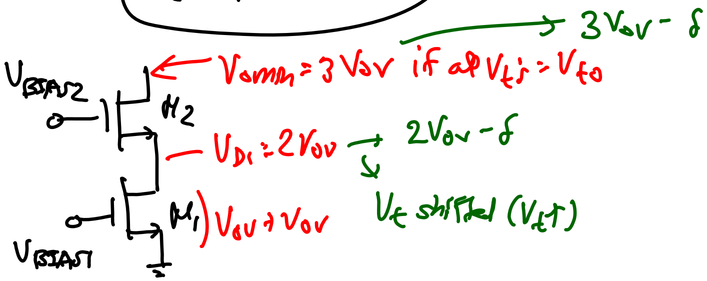
Problem: too much die area consumed when giving these devices their own wells $\rightarrow$ cost$\uparrow$

② Bias M_4 so that $V_{GS4} \geq V_t + 2V_{ov}$

e.g., $V_{GS4} = V_t + 3V_{ov}$

$$\left(\frac{W}{L}\right)_4 = \frac{1}{9}\left(\frac{W}{L}\right)_3$$

safety margin against V_t shift



Issues: $I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_t)^2(1 + \lambda V_{DS})$

(a)

channel length $\downarrow \rightarrow \lambda \uparrow$

If $V_{DS1} \neq V_{DS3}$

$$I_o = \frac{(1 + \lambda V_{DS1})}{(1 + \lambda V_{DS3})} I_{ref} \rightarrow I_o \neq I_{ref}$$

(b) As technology advances, $V_{DD} \downarrow \rightarrow$ losing headroom even for V_{BIAS}-generation

this is too much!

* → Solution → *

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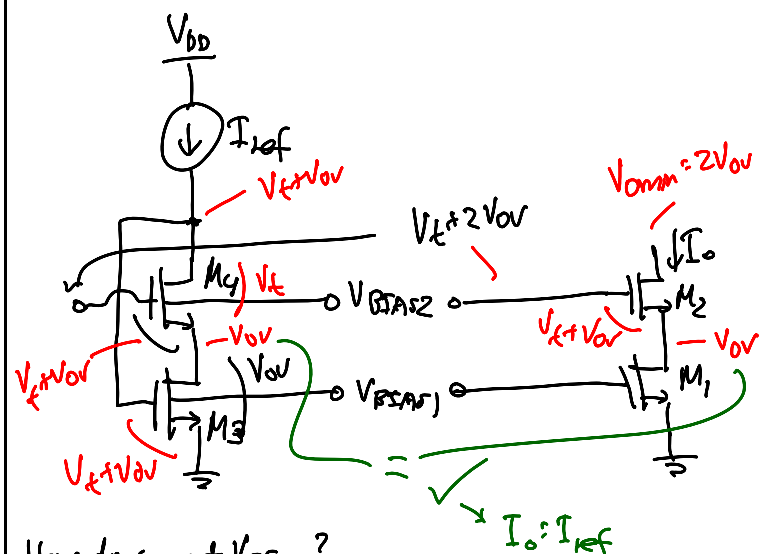
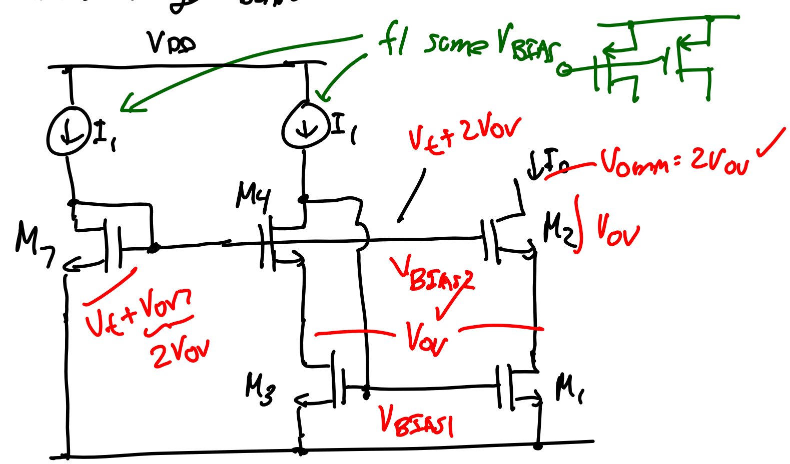
Solution: $\boxed{\text{Alternate Biasing Scheme for Cascode}}$



How do we get V_{BIAS2}?



$I_{D7} = I_{D3}$

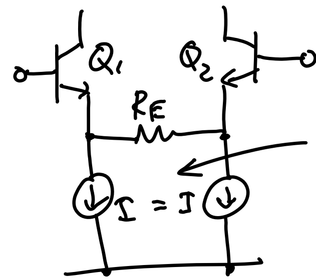
$$\cancel{\tfrac{1}{2}\mu_n C_{ox}}\left(\tfrac{W}{L}\right)_7 (\cancel{2}V_{ov})^2 = \cancel{\tfrac{1}{2}\mu_n C_{ox}}\left(\tfrac{W}{L}\right)_3 (\cancel{V_{ov}})^2 \quad 4$$

$$\boxed{\left(\tfrac{W}{L}\right)_7 = \tfrac{1}{4}\left(\tfrac{W}{L}\right)_3 = \tfrac{1}{4}\left(\tfrac{W}{L}\right)_{rest}}$$

rest of Xsistors

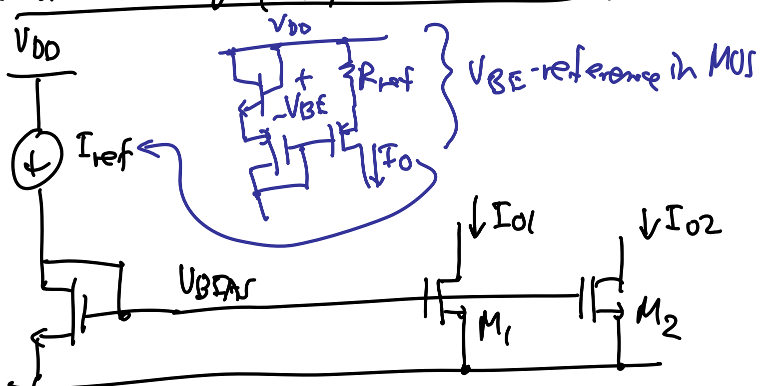
Note: Still must worry about Body effect!
→ defensive design → $V_{GS7} > V_t + 2V_{ov}$

Current Source Matching Considerations



Need equal currents to minimize common mode effects.

Consider matching of simple current sources:



In MOS, we need matched current sources:

$I_{o1} = I_{o2} \rightarrow I_{D1} = I_{D2}$

$I_{o1} = I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{t1})^2$

$I_{o2} = I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{t2})^2$

$I_{o1} \neq I_{o2}$ if $\underbrace{(W/L)_1 \neq (W/L)_2 \ \& \ V_{t1} \neq V_{t2}}$

will always have this due to finite fabrication tolerances!

Need to quantify their impact → How much mismatch in I_{o1} & I_{o2} is caused by

Define average & mismatch quantities,

Average	Mismatch
$I_D = \frac{1}{2}[I_{D1} + I_{D2}]$	$\Delta I_D = I_{D1} - I_{D2}$
$\frac{W}{L} = \frac{1}{2}\left[\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2\right]$	$\Delta\left(\frac{W}{L}\right) = \left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2$
$V_t = \frac{1}{2}[V_{t1} + V_{t2}]$	$\Delta V_t = V_{t1} - V_{t2}$

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$\frac{\Delta I_D}{I_D} \triangleq$ fractional current mismatch

$\frac{\Delta(W/L)}{(W/L)} \triangleq$ " (W/L) "

$\frac{\Delta V_t}{V_t} \triangleq$ " V_t "

Rearranging:

$I_{D1} = I_D + \frac{\Delta I_D}{2}$ | $(W/L)_1 = (W/L) + \frac{\Delta(W/L)}{2}$ | $V_{t1} = V_t + \frac{\Delta V_t}{2}$

$I_{D2} = I_D - \frac{\Delta I_D}{2}$ | $(W/L)_2 = (W/L) - \frac{\Delta(W/L)}{2}$ | $V_{t2} = V_t - \frac{\Delta V_t}{2}$

Plug these into the current equation:

$$I_{D1} = \cancel{I_D} + \frac{\Delta I_D}{2}$$

$$= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{t1})^2$$

$$= \frac{1}{2}\mu_n C_{ox}\left[\left(\frac{W}{L}\right) + \frac{\Delta(W/L)}{2}\right]\left[\underbrace{V_{GS} - V_t}_{V_{ov}} - \frac{\Delta V_t}{2}\right]^2$$

neg!

$$= \frac{1}{2}\mu_n C_{ox}\left[\left(\frac{W}{L}\right) + \frac{\Delta(W/L)}{2}\right]\left[V_{ov}^2 - 2V_{ov}\frac{\Delta V_t}{2} + \cancel{\frac{(\Delta V_t)^2}{4}}\right]$$

neg!

$$= \frac{1}{2}\mu_n C_{ox}\left[\left(\frac{W}{L}\right)V_{ov}^2 + \frac{\Delta(W/L)}{2}V_{ov}^2 - \left(\frac{W}{L}\right)V_{ov}V_t - \cancel{\frac{\Delta(W/L)}{2}V_{ov}\Delta V_t}\right]$$

$$= \underbrace{\cancel{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{ov}^2}}_{I_D} + \frac{1}{2}\mu_n C_{ox}V_{ov}^2\underbrace{\left[\frac{\Delta(W/L)}{2} - \frac{(W/L)}{V_{ov}}\Delta V_t\right]}_{\text{factor out } (W/L)}$$

$$\frac{\Delta I_D}{2} = \overbrace{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{ov}^2}^{I_D}\left[\frac{1}{2}\frac{\Delta(W/L)}{(W/L)} - \frac{\Delta V_t}{V_{ov}}\right]$$

$$\therefore \quad \frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{(W/L)} + \frac{\Delta V_t}{(V_{ov}/2)}$$

(−) sign means nothing, since ΔV_t could be (−)

Fractional Current Mismatch

Geometry-Based Component ↓ Indep of Bias Pt. Dep. on Fab!

$V_{ov}\uparrow$ → to minimize this component

With today's ckts: (driven by power savings for digital ckts.)

$V_{DD}\downarrow \to V_{ov}\downarrow \to \frac{\Delta I_D}{I_D}\uparrow$ X — Bad!

To combat this: $\left(\frac{W}{L}\right)\uparrow \to \frac{\Delta(W/L)}{(W/L)}\downarrow \to \frac{\Delta I_D}{I_D}\downarrow$

cost↑

Chip Size Over Time: