Lecture 23: Slew Rate (Revisited & Settling Time)

- Announcements:
- Design Project Checkpoint:
  - Due Tuesday, Nov. 19, 11:59 p.m.
  - Send to your TA a spice file for your op amp design that simulates correctly, i.e., that reaches a stable bias point where all transistors are saturated (except MOS R's)
  - It doesn't need to meet the project specs, but it should simulate correctly
- HW#10 due tomorrow @ 8 a.m.
- HW#11 online soon, due Nov. 27 @ 8 a.m.
- No homework over Thanksgiving
- Pre-Lecture for Settling Time online
- Lecture Topics:
  - Nulling the RHP Zero (finish)
  - Lab#3 Hints
  - Slew Rate (revisited)
  - Settling Time
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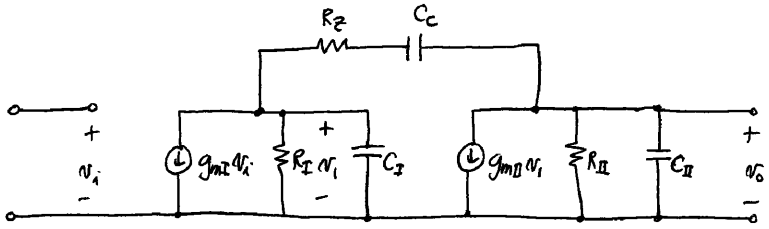
- Last Time:

Nulling Resistor in Series w/ C_c



Doing KCL:

$$p_1 = -\frac{1}{g_{mII}R_I R_{II} C_c}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_I C_{II} + C_c(C_I + C_{II})} \cong -\frac{g_{mII}}{C_{II}}$$

} same as before

$p_3 = -\frac{1}{R_Z C_I}$ ← pole due to R_Z

$z_1 = \frac{1}{C_c\left(\frac{1}{g_{mII}} - R_Z\right)}$ ← relocated zero (function of R_Z)

Note: The position of the zero depends upon the value of the "nulling resistor" R_Z

If $R_Z < \frac{1}{g_{mII}}$ then z_1 is in the RHP

If $R_Z > \frac{1}{g_{mII}}$ then " " LHP!

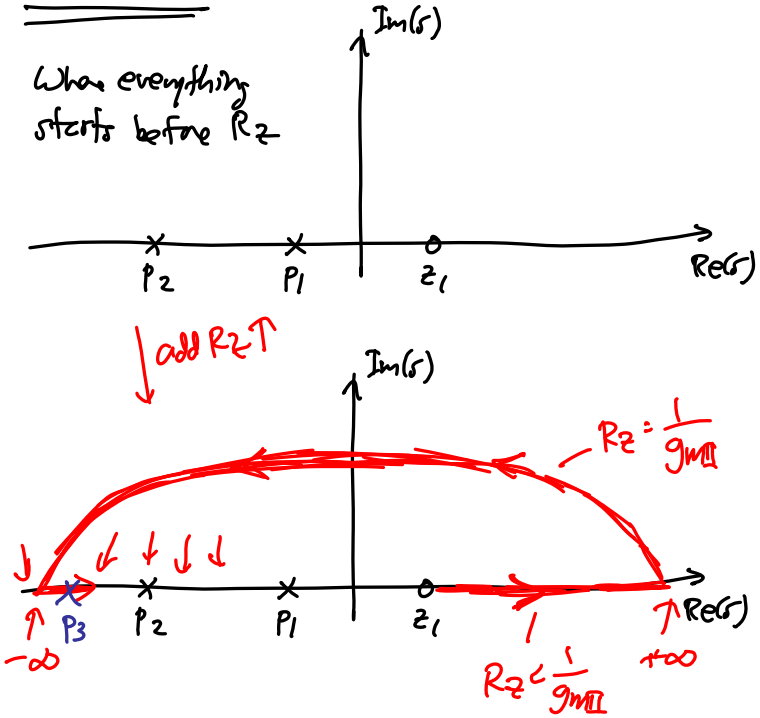
↳ This is great! → can convert the zero to a LHP one!
can even stick the zero on top of a pole to eliminate it!

$H(s) = \cdots \frac{(s - z_1)}{(s - p_1)}$

if $z_1 = p_1$

The Root Locus:

When everything starts before R_Z



Zero Placement Strategies:

① Eliminate z_1 → move it to ∞.

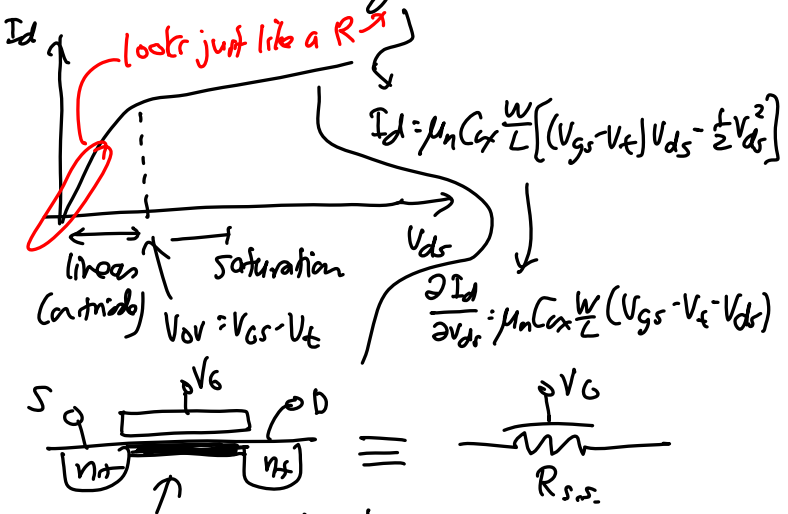
② Eliminate p_3 by placing z_1 on top of it.

③ Eliminate p_2 by placing z_1 on top of it.

Actual Implementation:

⇒ resistors are too big! → ∴ implement using a much smaller MOS resistor

MOS Resistor: just an MOS transistor operated in the linear region



uniform inversion charge → just like n+ material

control effective sheet R by Δ'ing gate voltage V_G

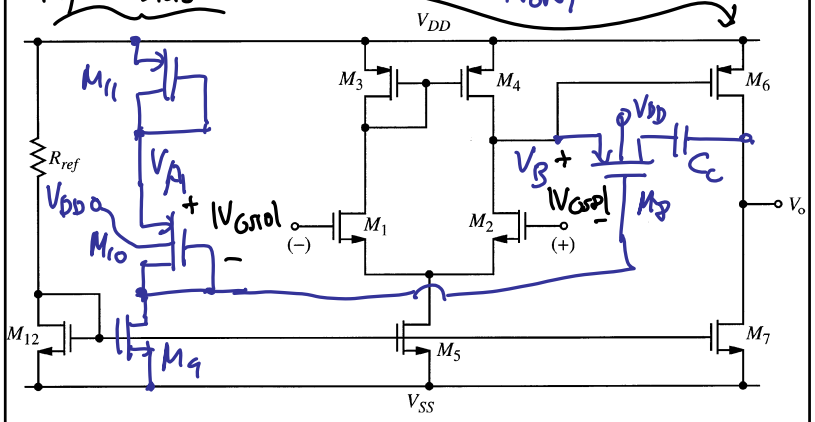
$$R_{s.s.} = \left[\frac{dI_d}{dV_{ds}}\right]^{-1}_{V_{GS}=V_{GS},\,V_{ds}=V_{DS}} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t-V_{DS})} = \frac{1}{g_{ds}}$$

variable resistor controllable by V_{GS}!

Actual Implementation

$V_{DSB} = 0V \Rightarrow R_B = \dfrac{1}{\mu_p C_{ox}(W/L)_B (|V_{GSB}| - |V_{tB}|)}$, $|V_{OVB}|$

Replica Bias



Design:

Need $V_A = V_B \rightarrow |V_{GS11}| = |V_{OS6}|$, know $|V_{t11}| = |V_{t6}|$

$$\sqrt{\frac{2I_{D11}}{\mu_p C_{ox}(W/L)_{11}}} = \sqrt{\frac{2I_{D6}}{\mu_p C_{ox}(W/L)_6}}$$

$$\Downarrow$$

$$\boxed{\left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_6 \frac{I_{D11}}{I_{D6}} = \left(\frac{W}{L}\right)_6 \frac{I_{D10}}{I_{D6}}}$$

Also need $|V_{GS10}| = |V_{GSB}|$

Because $V_A = V_B \rightarrow V_{S10} = V_{SB} \rightarrow |V_{t10}| = |V_{tB}|$

$$\therefore |V_{OV10}| = |V_{OVB}| = \sqrt{\frac{2I_{D10}}{\mu_p C_{ox}(W/L)_{10}}}$$

Thus:

$$R_B = \frac{1}{\mu_p C_{ox}(W/L)_B \sqrt{\dfrac{2I_{D10}}{\mu_p C_{ox}(W/L)_{10}}}} = \frac{\sqrt{\mu_p C_{ox}(W/L)_{10}}}{\mu_p C_{ox}(W/L)_B \sqrt{2I_{D10}}}$$

Case: Eliminate p_2 by placing z_1 on top of it.

$$R_Z = \frac{C_C + C_L}{g_{m6} C_C} = \frac{\sqrt{\mu_p C_{ox}(W/L)_{10}}}{\mu_p C_{ox}(W/L)_B \sqrt{2I_{D10}}}$$

$$g_{m6} = \sqrt{2\mu_p C_{ox}(W/L)_6 I_{D6}}$$

$$\Downarrow$$

$$\boxed{\left(\frac{W}{L}\right)_B = \sqrt{\left(\frac{W}{L}\right)_6 \left(\frac{W}{L}\right)_{10} \frac{I_{D6}}{I_{D10}} \cdot \left(\frac{C_L}{C_C + C_L}\right)}}$$

Case: Move $z_1 \rightarrow \infty$.

$$R_Z = \frac{1}{g_{m6}} \Rightarrow \boxed{\left(\frac{W}{L}\right)_B = \sqrt{\left(\frac{W}{L}\right)_6 \left(\frac{W}{L}\right)_{10} \frac{I_{D6}}{I_{D10}}}}$$

Project Design → Lab #3

Ad Hoc Procedure:

① Write down all equations for all needed specs.
↳ then study the dependencies, e.g.,

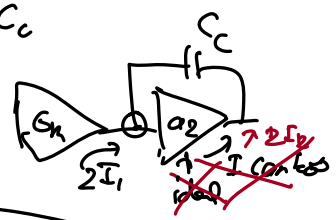
a_0 = gain = $f(I_d, \lambda, ..) \sim \frac{1}{\sqrt{I_d}}$

⋮

② Choose C_c

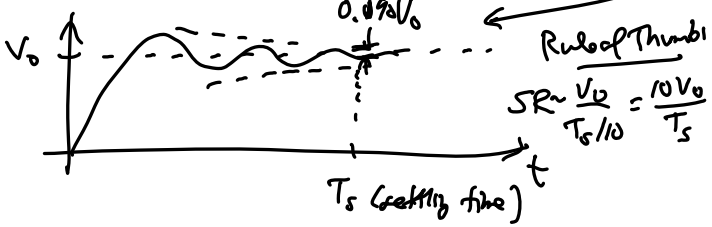
ω_u = unity gain freq. : $\frac{g_{m1}}{C_c}$

$|p_2| \cong \frac{g_{m2}}{C_L}$



③ Choose I_d's → SR

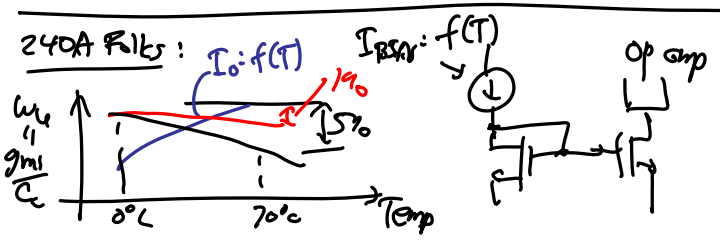
④ Determine $\frac{W}{L}$'s (Governed by swing & input range)



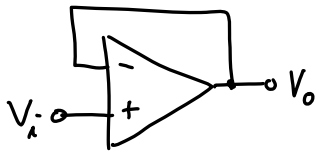
Rule of Thumb:

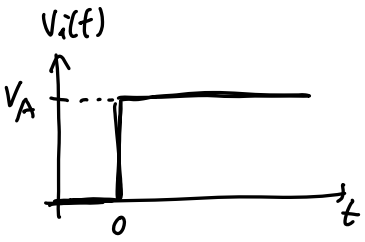
$SR \sim \frac{V_o}{T_s/10} = \frac{10 V_o}{T_s}$

240A Rik's:



Slew Rate (f/ before)





Using Laplace Xform Theory:

$\frac{V_o}{V_i}(s) = \frac{1}{1+\frac{s}{\omega_1}} = \frac{1}{1+s\tau_1}$

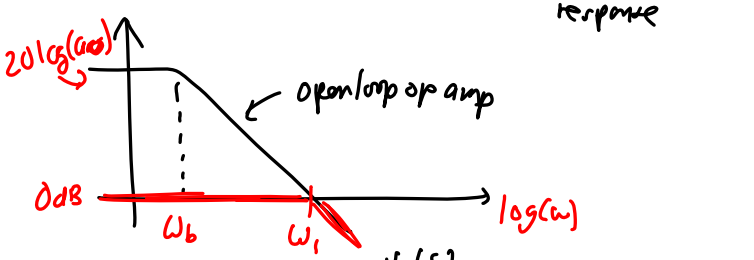
≈ single (dominant) pole

$V_i(s) = \frac{V_A}{s}$

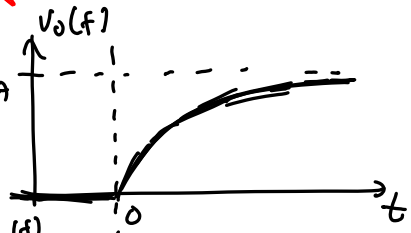
$V_o(s) = \frac{V_A}{s(1+s\tau_1)} = \frac{V_A}{s} - \frac{V_A}{s+\frac{1}{\tau_1}}$

⇕ Inverse Laplace Xform

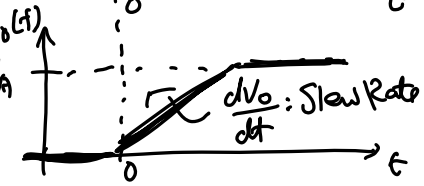
$V_o(t) = V_A(1-e^{-t/\tau_1})$ ← expected response



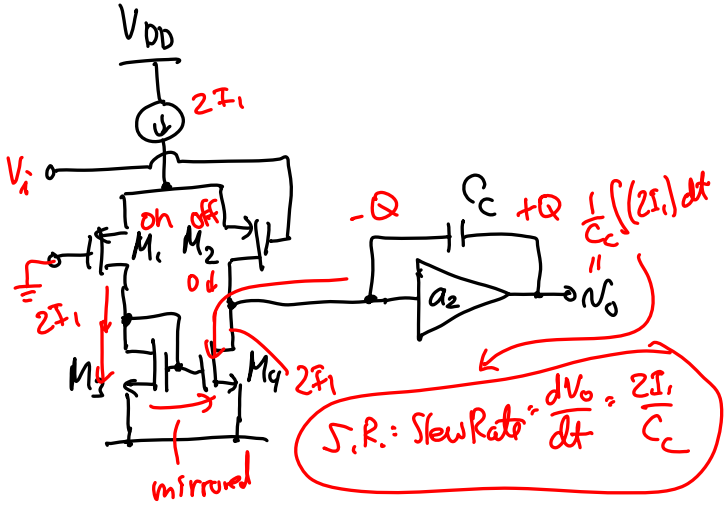
Expectation:



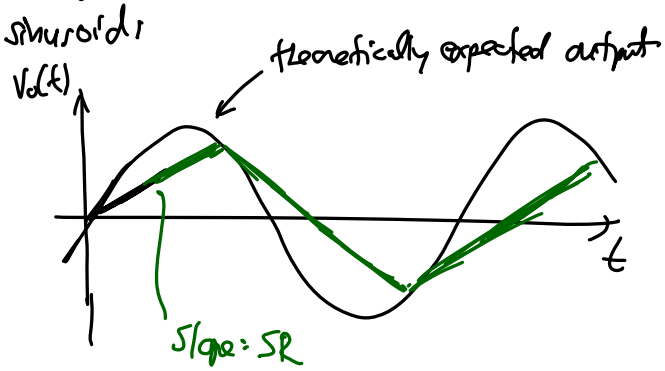
What we really see from a real op amp:



Reason: 1st or 2nd stage of op amp cannot source enough current to mimic the slope (or speed) of a fast rising input signal



If apply a very fast (i.e., high frequency), large amplitude sinusoid:



In terms of design variables:

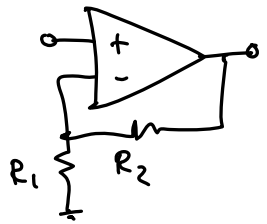
$$S.R. = \frac{dV_o}{dt} = \frac{I_{xmax}}{C_c} = \frac{I_{xmax}}{G_{m1}} \omega_{ugA} A_o = S.R.$$

$$C_c = \frac{G_{m1}}{\omega_{ugA} A_o} \leftarrow \text{closed loop gain}$$

ω_{ugA}: ω @ $|T(j\omega)| = 1$

To Increase S.R.:

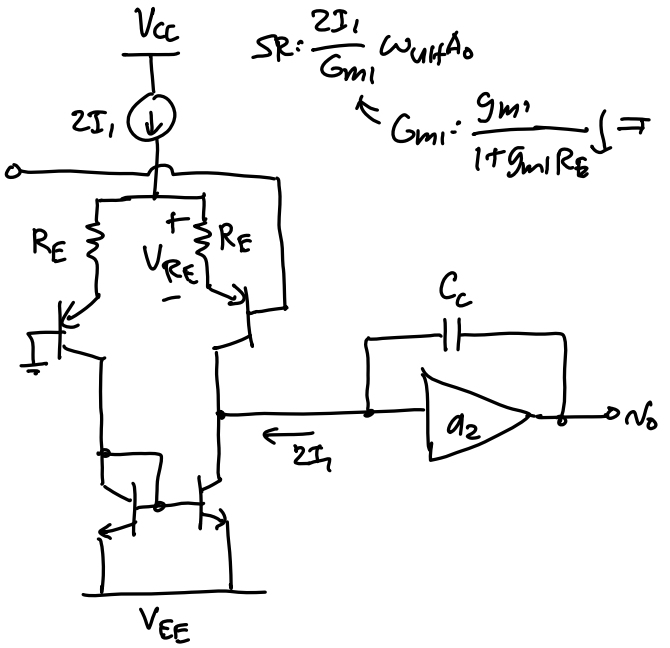
1. Decrease G_{m1} ✓
2. Increase ω_{ugA} → increase ω_2 → limited by the MOSFET freq. range
3. Use a larger A_o, if possible. (A_o ↑ closed loop gain; only if permitted by the application)



$$A_o = 1 + \frac{R_2}{R_1}$$

Increasing S.R. via G_m-Reduction

① Emitter or Source Degeneration of the Input Stage:



$SR: \frac{2I_1}{G_{m1}} \omega_{ugf} A_0$

$G_{m1}: \frac{g_{m1}}{1+g_{m1}R_E}$ ⇒ SR↑

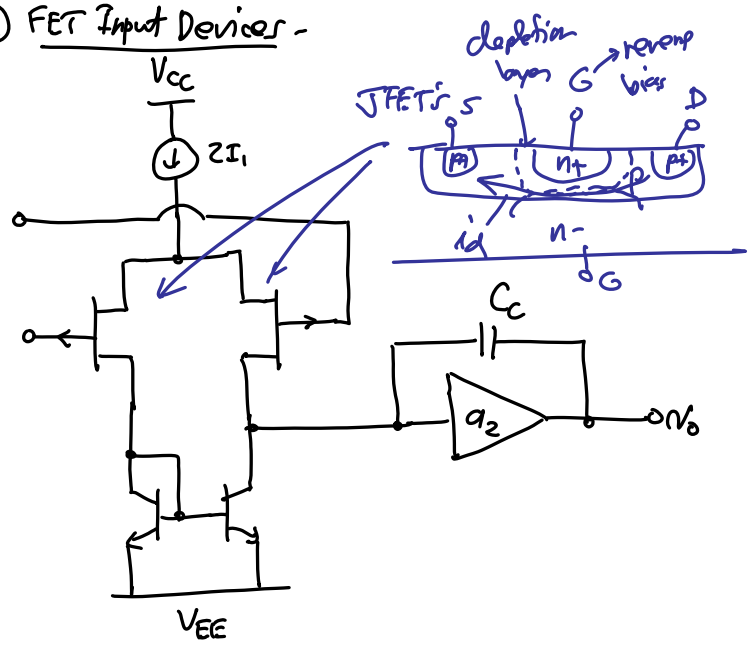
Limitations:

① R_E mismatch → V_{os}
↳ must limit V_{RE} to limit V_{os}

② R_E↑ → gain↓ (SR-gain trade-off)

③ R_E contributes thermal noise → must limit the size of R_E to preserve op amp noise performance

② FET Input Devices -



For FETs: $\frac{g_m}{I_D} \cong \frac{2}{V_{GS}-V_t}$ ← ≈0.2V

For bipolar: $\frac{g_m}{I_C} = \frac{1}{V_T}$ ← 26mV

$\frac{\text{FET S.R.}}{\text{BJT S.R.}} = \frac{\frac{I_D}{g_{mF}}\omega_{ugf}}{\frac{I_C}{g_{mB}}\omega_{ugf}} = \frac{\frac{V_{GS}-V_t}{2}}{V_T} = \frac{V_{GS}-V_t}{2V_T} \approx \frac{260}{26} \approx 10$

Limitations:

① Higher V_{os}.
② Increased voltage noise. → (but decreased current noise)

Settling Time

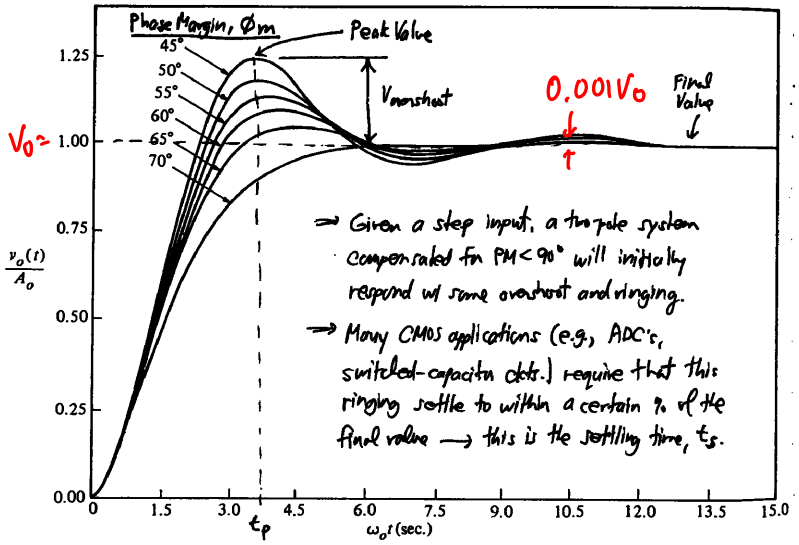


Figure 8.2-3 Response of second-order system with various phase margins.

Obtain Expressions fn:

① $V_{overshoot}$
② Settling Time, T_s

} as functions of phase margin, ϕ_m

- Go through settling time handout