Lecture 24: PSRR & Feedback I

- Announcements:
- HW#11 due Nov. 27 @ 8 a.m.
- No homework over Thanksgiving
- Pre-Lecture for Settling Time online
- Lecture Topics:
  - Settling Time (finish)
  - Power Supply Rejection Ratio (PSRR)
  - Start Feedback
- ---------------------------------------
- Last Time: going thru Settling Time Handout

Settling Time

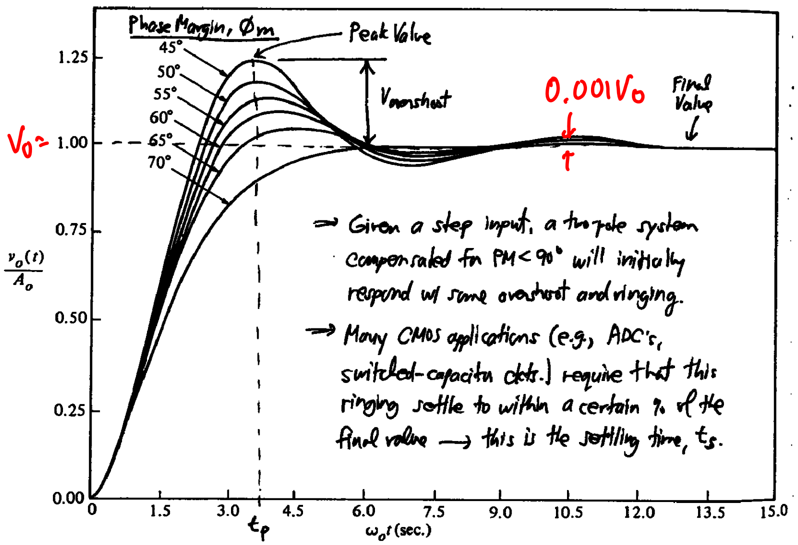


Figure 8.2-3 Response of second-order system with various phase margins.

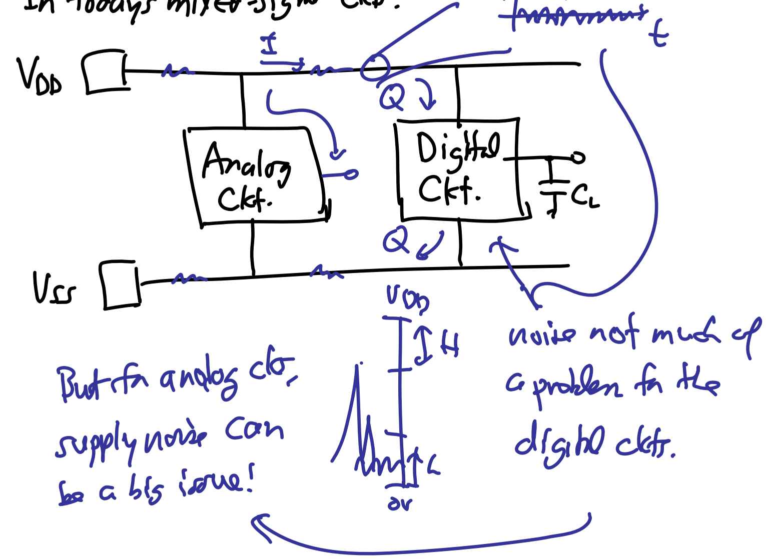
Obtain Expressions for:

① $V_{overshoot}$
② Settling Time, T_s

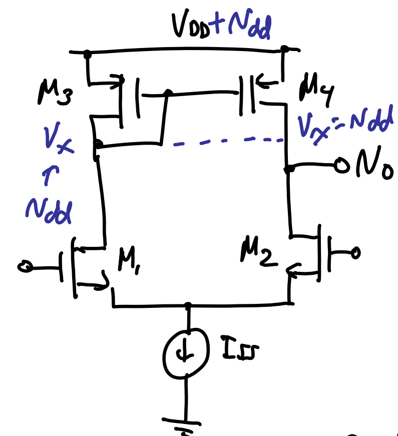
} as functions of phase margin, ϕ_m

Power Supply Rejection Ratio (PSRR)

In today's mixed-signal ckts:



Ex. CMOS Differential Input Stage w/ Current Mirror Load



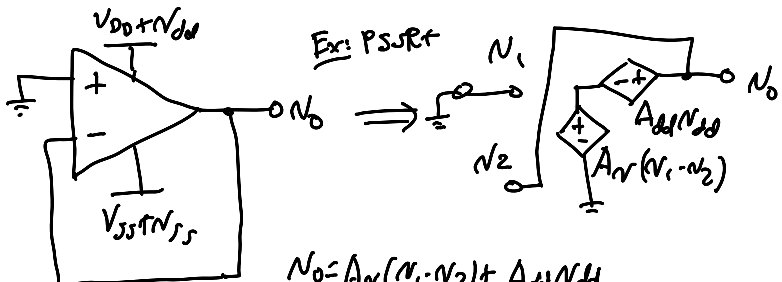
$\frac{N_o}{N_{dd}} \approx 1 \Rightarrow$ supply noise directly seen @ output!

For this example, $PSRR \cong \frac{g_{m2}(r_{o2}||r_{o4})}{1} = g_m(r_{o2}||r_{o4})$

Definition. Power Supply Rejection Ratio (PSRR)

$$PSRR \triangleq \frac{\text{Gain f/ Input to Output}}{\text{Gain f/ Supply to Output}} = \frac{A_v|_{v_{dd}=0}}{A_{dd}|_{v_i=0}}$$

For more complicated ckts., much more work is req'd.
↳ to make it easier, use a unity gain configuration
↳ can also get $PSRR = f(\omega)$



$v_o = A_v(v_1 - v_2) + A_{dd}v_{dd}$, where $v_2 = v_o$

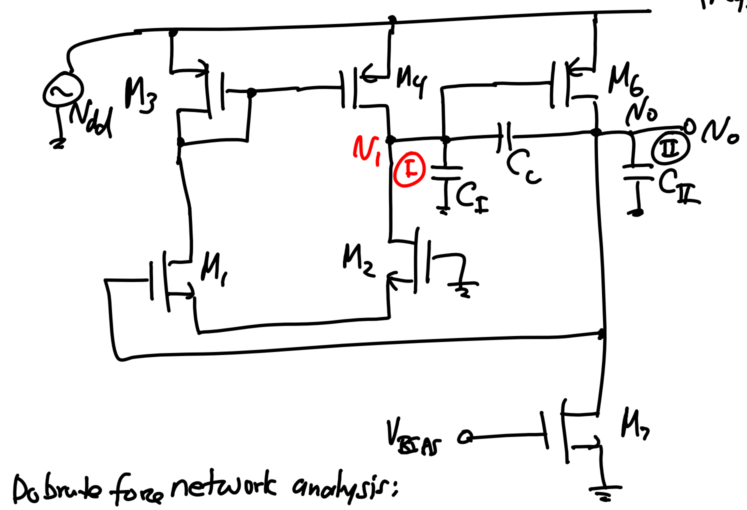
$$v_o(1+A_v) = A_{dd}v_{dd} \rightarrow \frac{v_o}{v_{dd}} = \frac{A_{dd}}{1+A_v} = \frac{1}{\frac{A_v}{A_{dd}}} \approx \frac{1}{PSRR^+}$$

$$\boxed{\frac{1}{PSRR^+} = \frac{v_o}{v_{dd}}} \rightarrow \boxed{PSRR^+ = \frac{v_{dd}}{v_o}}$$

↗ Just find this Xfer fcn to get PSRR+ when the op amp is hooked in unity gain!

Two-Stage Op Amp PSRR+

Want $PSRR^+ = f(\omega)$ ← freq.



Do brute force network analysis:

KCL (I): $G_I v_{dd} = (G_I + sC_c + sC_I)v_1 - (g_{mI} + sC_c)v_o$

KCL (II): $(g_{mII} + g_{ds6})v_{dd} = (g_{mII} - sC_c)v_1 + (G_{II} + sC_c + sC_{II})v_o$

$G_I = g_{ds1} + g_{ds4} = g_{ds2} + g_{ds4}$
$G_{II} = g_{ds6} + g_{ds7}$
$g_{mI} = g_{m1} = g_{m2}$
$g_{mII} = g_{m6}$

$\left[g_{ds} = \frac{1}{r_o}\right]$ ← For saturated device.

math & rearranging

Get:

$$\left(\frac{v_{dd}}{v_o}\right)\bigg|_{closed\text{-}loop} = \frac{N(s)}{D(s)} = \frac{(\quad)}{(\quad)} \quad \text{polynomials}$$

↳ then use: $N(s) = 1 + \left(\frac{s}{z_1} + \frac{s}{z_2}\right) + \frac{s^2}{z_1 z_2} \approx 1 + \frac{s}{z_1} + \frac{s^2}{z_1 z_2}$

$$PSRR^+ = A_{vo}^+ \left[\frac{\left(1+\frac{s}{GB}\right)\left(1+\frac{s}{|p_2|}\right)}{\left(1+\frac{s}{GB/A_{vo}^+}\right)}\right]$$

where GB = Gain BW Product $= \frac{g_{mI}}{C_c}$

A_{vo}^+ = DC $PSRR^+ = \frac{g_{mI}\, g_{mII}}{G_I\, g_{ds6}}$

$|p_2| = \frac{g_{mII}}{C_{II}}$ $\qquad \omega_p^+ = \frac{GB}{A_{vo}^+}$

To maximize $PSRR^+$: (@dc) decrease g_{ds6}, raise g_{mII}

$$PSRR^- = A_{vo}^- \left[\frac{\left(1+\frac{s}{GB}\right)\left(1+\frac{s}{|p_2|}\right)}{\left(1+\frac{s}{\omega_{p^-}}\right)}\right]$$

where $A_{vo}^- = \frac{g_{mI}\, g_{mII}}{G_I\, g_{ds7}}$

$GB = \frac{g_{mI}}{C_c}$ $\qquad \omega_p^- = \frac{G_I}{C_c + C_I} \approx \frac{G_I}{C_c}$

$|p_2| = \frac{g_{mII}}{C_{II}}$

To maximize $PSRR^-$: ① decrease g_{ds7}
② increase $g_{mII} = g_{m6}$

Remarks.

① Since often $g_{ds7} < g_{ds6}$ → often $PSRR^- > PSRR^+$ (@dc) [red note: $r_{o7} = \frac{1}{g_{ds7}}$]

② $\frac{\omega_p^-}{\omega_p^+} = \frac{G_I/C_c}{\frac{G_I\, g_{ds6}}{g_{mII}\, C_c}} = \frac{g_{mII}}{g_{ds6}}$ → that's quite large
$\therefore \omega_p^- \gg \omega_p^+$

Thus, for an NMOS input op amp, $PSRR^-$ is often better than $PSRR^+$. → in design, need to worry more about $PSRR^+$!

③ Some methods for ~~reducing~~ maximizing PSRR:

(i) Use buffer-based zero-cancellation in the compensation loop.

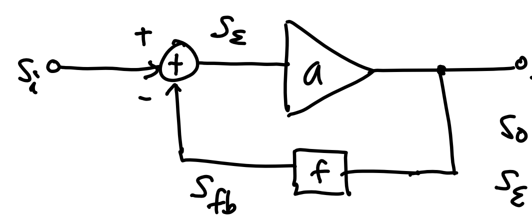
(ii) Use cascode circuitry, or balanced circuit topologies.

(iii) Supply-independent biasing.

(iv) Design strategies to minimize parasitic capacitive feedthrough.

Feedback

⇒ we know this:



$S_o = a S_\varepsilon$

$S_\varepsilon = S_i - f S_o$

⇓

$$\boxed{\frac{S_o}{S_i} = \frac{a}{1+af} = A}$$

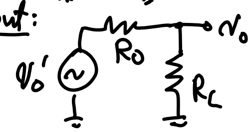
Benefits of Negative FB

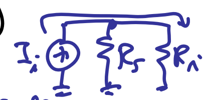
1. Stabilizes the gain of the amp against parameter changes & active device variations
2. Modifies R_i and R_o → basically improves their values according to the type of amplifier implemented

e.g., voltage amp: R_i: large, R_o: small

@ input: If R_i: large, $v_i \approx v_s$. ($R_i \gg R_s$)

@ output: If R_o = small, $v_o \approx v_o'$. ($R_o \ll R_L$)





current-to-voltage amp: R_i: small, R_o: small

voltage-to-current amp: R_i: large, R_o: large

current-to-current amp: R_i: small, R_o: large

3. Reduces distortion; improves linearity.
4. Increases bandwidth (ω_{-3dB}).

Disadvantages of Neg. FB

1. Gain is reduced → reduction factor ~ equal to the amount of gain stabilization, distortion reduction, etc...

Solution: Add more stages of gain → but this adds cost & power...

2. Feedback causes stability problems (if not compensated properly)

Gain Sensitivity Reduction Via FB

$$A = \frac{a}{1+af} \rightarrow \frac{dA}{da} = \frac{(1+af) - af}{(1+af)^2} = \frac{1}{(1+af)^2} \rightarrow \text{small}$$

↑ usually of this

For a Δ in op amp gain: δa

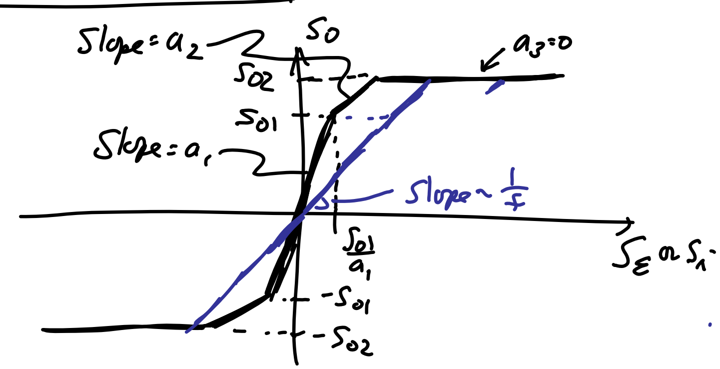
$$\frac{\delta A}{\delta a} = \frac{1}{(1+af)^2} \rightarrow \delta A = \frac{\delta a}{(1+af)^2}$$

↑ much smaller than δa

... and the fractional change:

$$\frac{\delta A}{A} = \frac{1+af}{a}\frac{\delta a}{(1+af)^2} \Rightarrow \boxed{\frac{\delta A}{A} = \frac{\frac{\delta a}{a}}{1+af}}$$

Distortion Reduction via FB



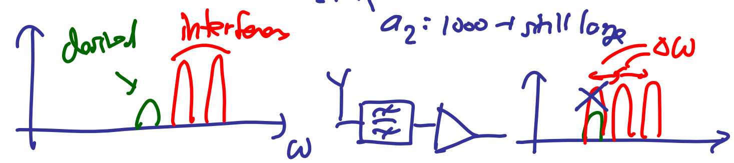
Now, close the loop: ← for a_1: large ≈ 20K

$0 < S_o < S_{o1}$: $A_1 = \frac{a_1}{1+a_1 f} \approx \frac{1}{f}$

$S_{o1} < S_o < S_{o2}$: $A_2 = \frac{a_2}{1+a_2 f} \approx \frac{1}{f}$

still linear over a larger range!

↑ a_2: 1000 → still large



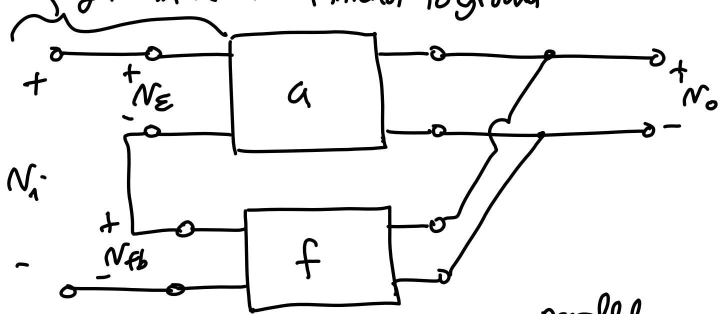
"Inspection" Analysis of FB Ckts.

↓ starts with...

Identification of FB Connection Types

Series Connection - FB network port in series w/ amplifier port

↳ must go thru both the FB port & the amplifier port to get from the node of interest to ground



Shunt Connection - FB network port in shunt (parallel) w/ amplifier port

↳ can get from the node of interest to ground via either FB network port or the amplifier port

↪ over