Lecture 3: Device Models II (bipolar & MOS)

- Announcements:
- HW#1 is online
- Discussion sections start this week
  - Discussion Section 102 Time and Location
  - F 4-5 p.m., 247 Cory
  - TA Office Hours will be held in 288 Cory
  - My OH: F 11:30-12:30
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- Lecture Topics:
  - Review (fast)
  - Bipolar Junction Transistor Modeling
    - Basic Structure & Physics
    - Large Signal Models
    - DC Operating Point
    - Small Signal Models
    - Frequency Shaping Elements
    - Layout
    - Unity Gain Frequency
  - MOS Transistor Modeling
    - Basic Structure & Physics
    - Large Signal Models
    - Threshold Voltage
    - Small Signal Models
    - Frequency Shaping Elements
    - Layout and Inclusion of Parasitics
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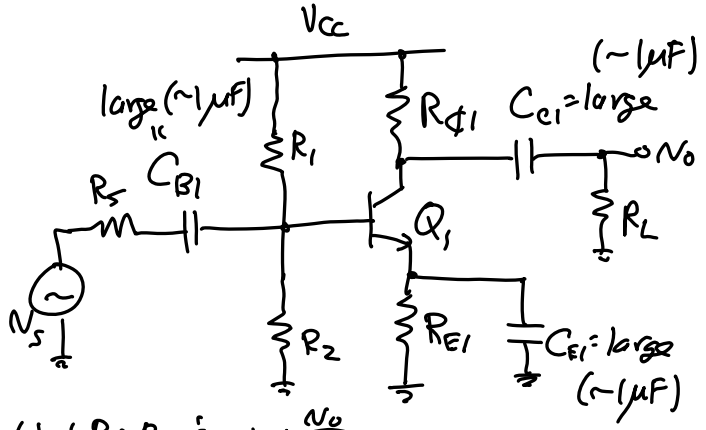
- Last Time: Reviewing BJT's and DC biasing using the handout
- Continue with this …

Procedure for Small-Signal Analysis

Ex. Discrete Common-Emitter Ckt.



Want R_i, R_o, & gain: $\frac{V_o}{V_s}$.

Procedure:

① Find the DC operating pt. → get voltages & currents at all nodes & branches, respectively.