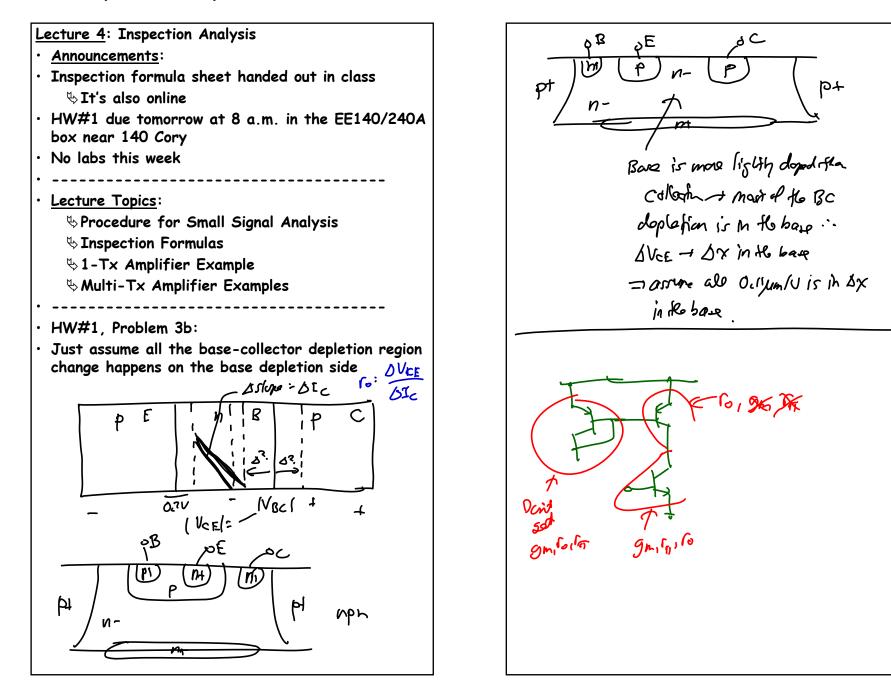
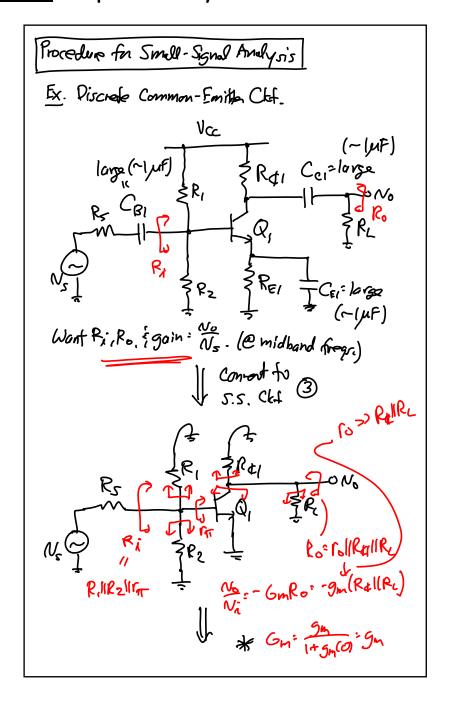
<u>EE 140/240A</u>: Analog Integrated Circuits <u>Lecture 4w</u>: Inspection Analysis

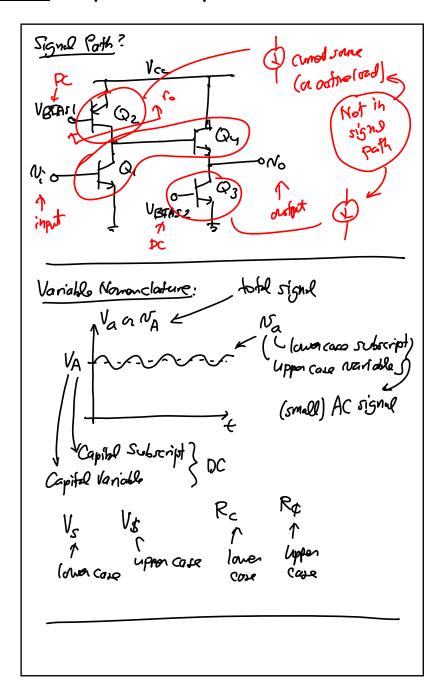


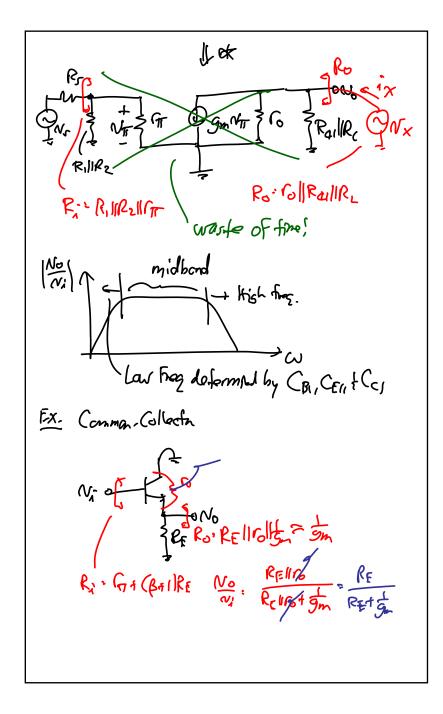
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Procedure: () Find the DC openations pt. → get woltages f Currents at all nodes & branches, respectively. 2 Determine S.S. parameter (i.e., elements) for dovies in the signer porth (e.g., gm, ru, etc.) 3 Convert the full clif. to the S. S. Clif. ⇒ zero out or sources ~ V -1 shout - short out large copecitions (FG) IF readed, replace the X sister or its small signed model (e.g., hybrid-TT model, T-model) > this should Not be node often = when is it needed ? -> generally, in color where the is feedback the without (46) Analyze by inspection (based on prior S.S. andysis experience !) This should be 9990 of the time!

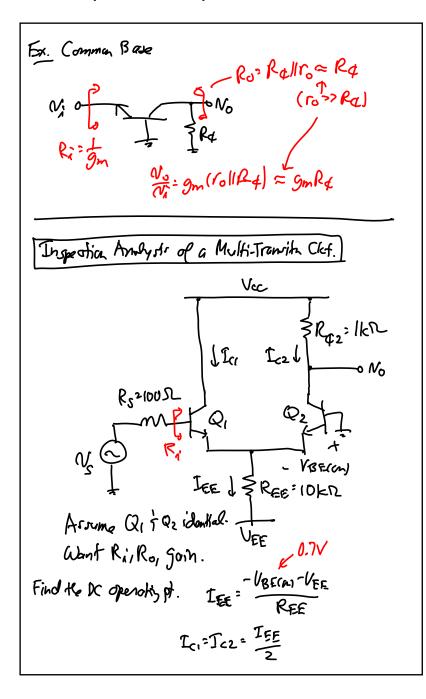
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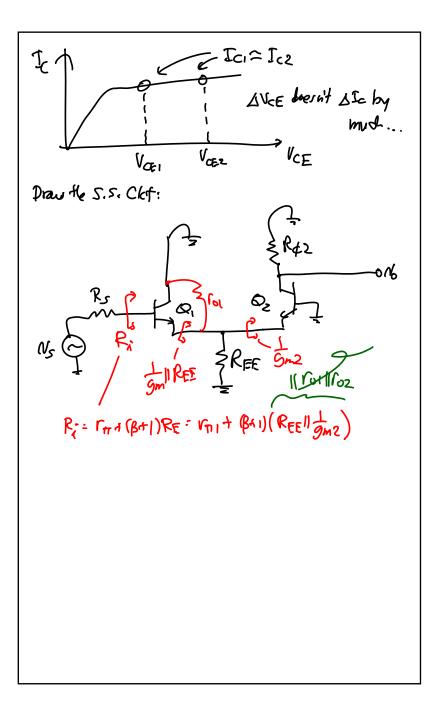




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