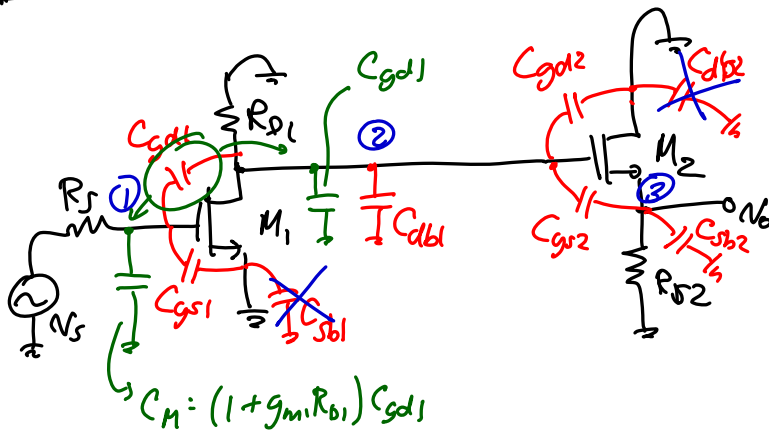


Lecture 7: Active Loads I

- Announcements:
- Lab 1 next week - report to your lab section
- HW#3 has been online
- Lecture Topics:
 - ↳ Open Ckt Time Constant (OCTC) Analysis (cont)
 - ↳ Short Ckt Time Constant (SCTC) Analysis
 - ↳ Example Low Freq. Response Determination
 - ↳ Active Loads
 - Why active loads?
 - Examples of actively loaded amplifiers

• Last Time:

MOS Two-Stage Amplifier



$$\tau_{D1} = [(1 + g_{m1} R_{D1}) C_{gd1} + C_{gs1}] R_S$$

$$\tau_{D2} = [C_{gd1} + C_{db1} + C_{gd2}] (R_{D1} \parallel R_{D2})$$

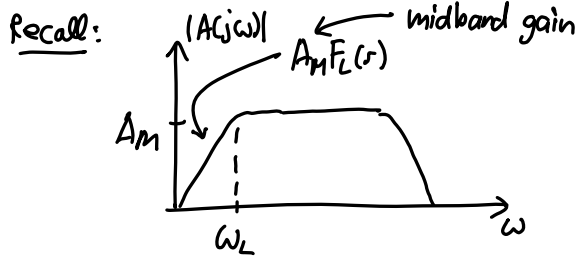
$$\tau_{D3} = C_{sb2} \left(\frac{1}{g_{m2} + g_{mb2}} \parallel R_{S2} \right)$$

~~$\tau_{gs2} = C_{gs2} \frac{(R_{D2} + R_{S2})}{(1 + (g_{m2} + g_{mb2}) R_{S2})}$~~ *Case neglect since the gain approx $C_{gs2} \sim 1$*

$\omega_H = \frac{1}{\tau_{D1} + \tau_{D2} + \tau_{D3} + \tau_{gs2}} \rightarrow f_H = \frac{\omega_H}{2\pi}$

Handwritten notes:
 $i=0$
 $N_x \rightarrow N_x$
 $\delta N = 0$
 $\rightarrow C$ not the

Low Freq. Amplifier Response Using Short Circuit Time Constant Analysis (SCTC)



In general, for the low freq. response:

$$F_L(s) = \frac{s^{n_z} + d_1 s^{(n_z-1)} + \dots}{s^{n_p} + e_1 s^{(n_p-1)} + \dots}, \quad n_z = \# \text{ poles} = \# \text{ zeros}$$

We can express the coefficient e_1 by:

$$e_1 = \omega_{p1} + \omega_{p2} + \dots + \omega_{pn}$$

For the case of a dominant pole:

↳ i.e., the highest freq. pole

$$F_L(s) \approx \frac{s}{s + \omega_L} = \frac{s}{s + e_1} \rightarrow e_1 \approx \omega_{p1} = \omega_L$$

$$\omega_L \approx e_1 = \sum_j \omega_{pj} = \sum_j \frac{1}{C_j R_{j,s}} = \sum_j \frac{1}{\tau_{j,s}}$$

where $C_j \triangleq$ various large ($> 10 \text{ nF}$) capacitors in the ckt. (e.g., the bypass caps.)

$R_{j,s} \triangleq$ driving point resistance seen between the terminals of C_j determined with:

For readability, can go to Sedra & Smith

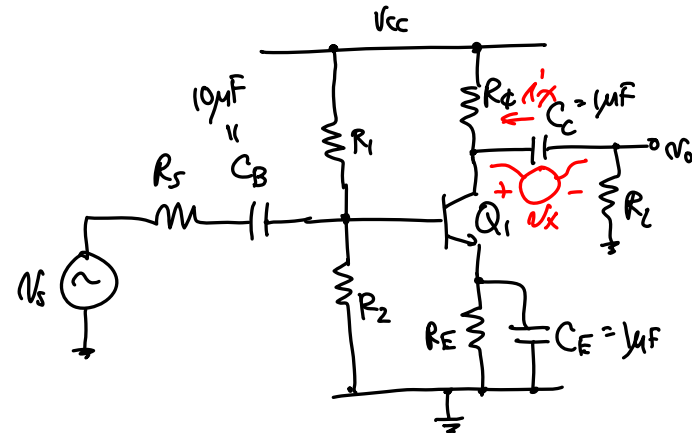
- all large capacitors short-circuited, except C_j , which is replaced by the test voltage source for R determination

- all independent sources eliminated (i.e., short voltage sources, open current sources)
- open all H.F. capacitors (i.e., small caps in the pF range, or $< 1 \text{ nF}$)

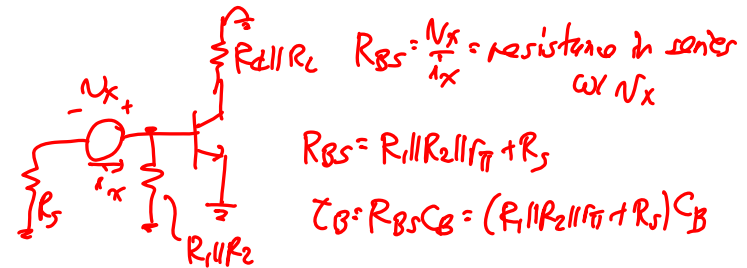
Again, for the case where there are no dominant poles, a reasonable approximation is:

$$\omega_L \approx \sqrt{\omega_{p1}^2 + \omega_{p2}^2 - 2\omega_{z1}^2 - 2\omega_{z2}^2}$$

Ex: Determine the L.F. response of the C.E. Amplifier



(a) ω_{pB} due to C_B : Short ckt. C_C & C_E



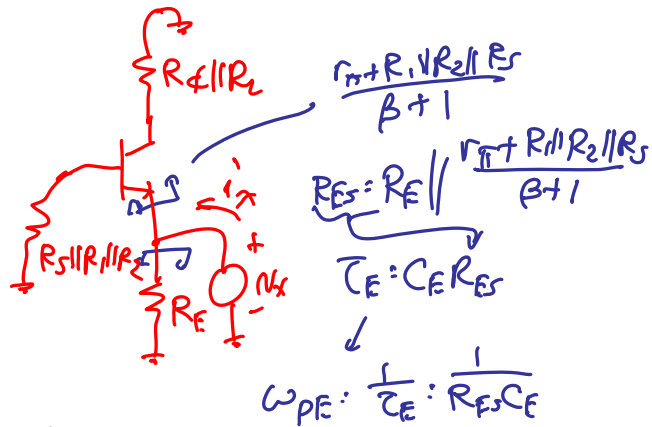
$$\therefore \omega_{pB} = \frac{1}{\tau_B} = \frac{1}{(R_1 \parallel R_2 \parallel V_T + R_S) C_B}$$

(b) ω_{pc} due to C_c : short C_B & C_E

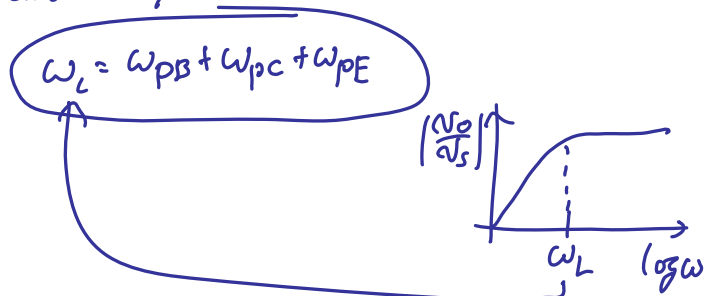
\Rightarrow again, R_{CS} = resistance in series w/ N_x
(seen fr both sides)

$$\tau_c = (R_{CS} \parallel R_E) C_c \rightarrow \omega_{pc} = \frac{1}{\tau_c} = \frac{1}{(R_{CS} \parallel R_E) C_c}$$

(c) ω_{pe} due to C_E : short C_B & C_c

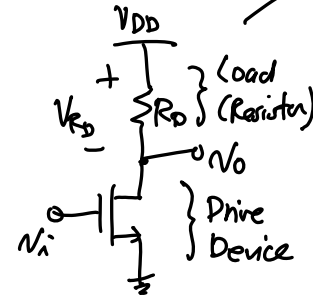


and finally:



Active Loads

\Rightarrow Why use them?



Gain: $\frac{v_o}{v_i} = -g_m R_D$

For $\frac{v_o}{v_i} \uparrow$, must:

① Raise $g_m \rightarrow$ raise I_D

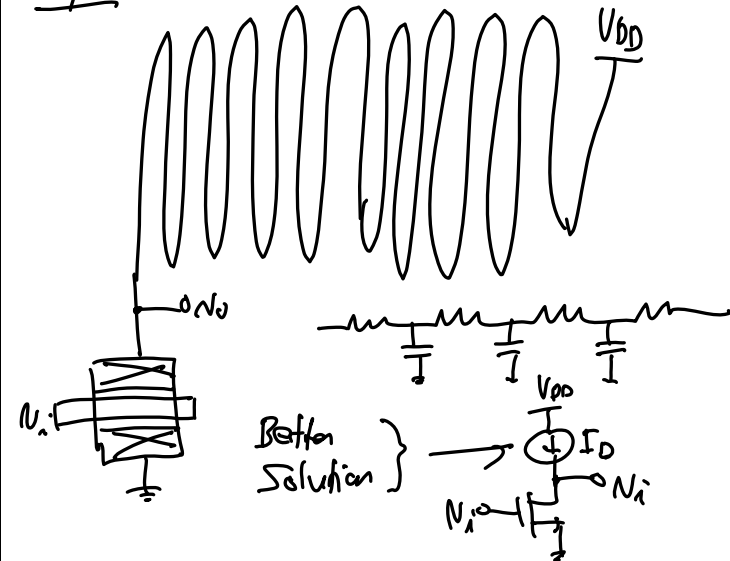
Problem: $V_{R_D} = I_D R_D \uparrow$

Limited by the supply V_{DD} !

② Raise $R_D \rightarrow$ as g_m, V_{R_D}

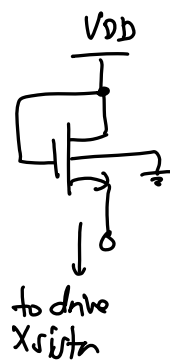
another problem: area consumption by R_D

Layout:



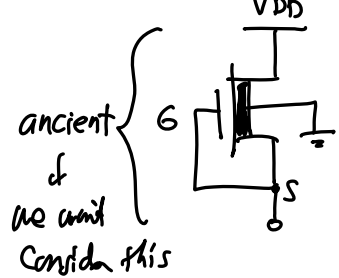
Types of Active Loads → current source

Diode-Connected Enhancement Load:
Load:



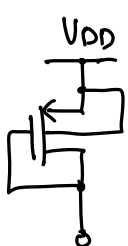
to drive Xsistn

Depletion Load:

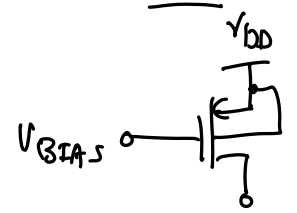


ancient & we won't consider this

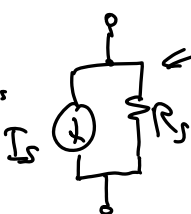
Diode-Connected PMOS Load:



PMOS Current Source Load:

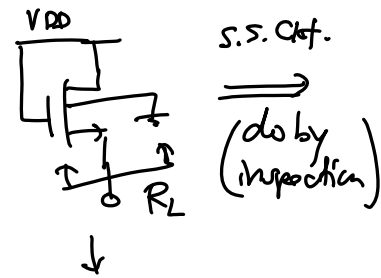


Norton Equivalent:



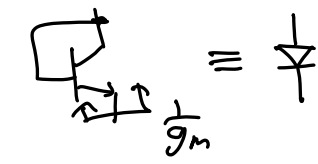
ideal when $R_s = \infty$

Diode-Connected Enhancement Load



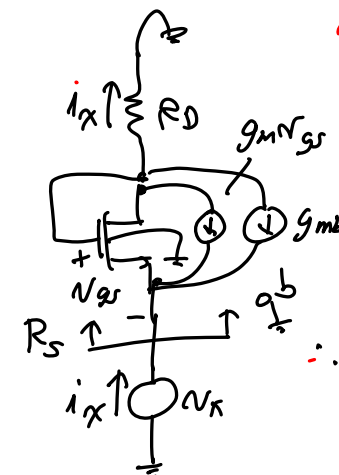
s.s. ckt.
(do by inspection)

"Diode-Connected"



$R_i = \frac{1}{g_m} \parallel \frac{1}{g_{mb}}$
 $= \frac{1}{g_m + g_{mb}}$
 $\sim 1-10k\Omega$

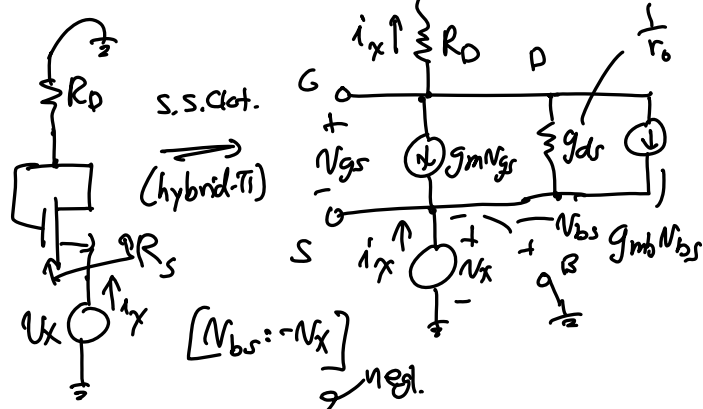
How about this?



$i_x = -g_m V_{gs} - g_{mb} V_{bs}$
 $= -g_m (i_x R_D - V_x) - g_{mb} (-V_x)$
 $= g_m V_x - g_m R_D i_x + g_{mb} V_x$
 $i_x (1 + g_m R_D) = (g_m + g_{mb}) V_x$
 $\therefore R_s = \frac{V_x}{i_x} = \frac{1 + g_m R_D}{g_m + g_{mb}}$
 $= \frac{\frac{1}{g_m} + R_D}{1 + \eta}$
 $[\eta = \frac{g_{mb}}{g_m}]$

Full hybrid- π analysis:

(in case you want to see it)



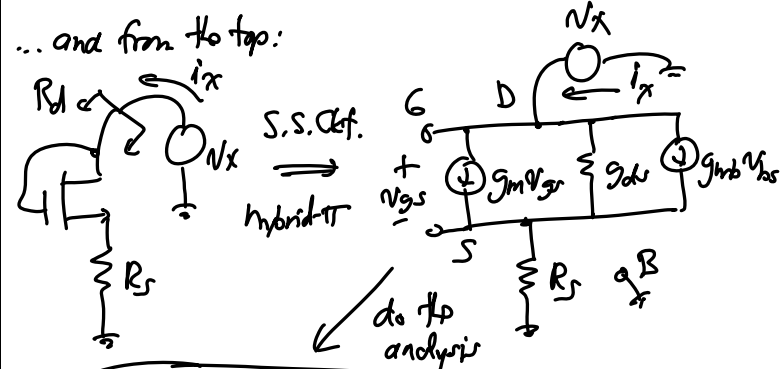
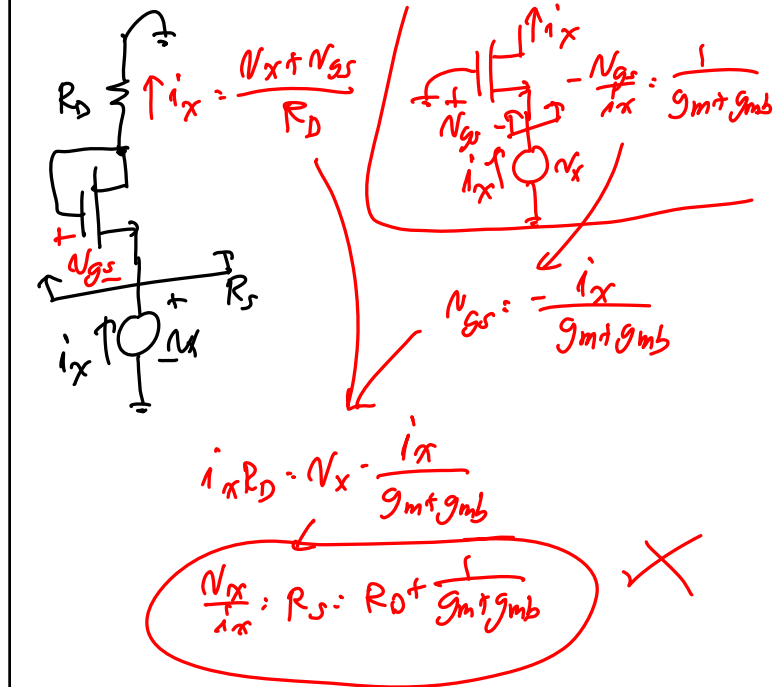
$$i_x = -g_m V_{gs} + g_{dr} (-V_{gs}) - g_{mb} V_{bs}$$

$$= g_m (V_x - i_x R_D) + g_{mb} V_x$$

$$R_S = \frac{V_x}{i_x} = \frac{1 + g_m R_D}{g_m + g_{mb}} = \frac{1}{g_m + g_{mb}} + \frac{R_D}{1 + \eta}$$

$$R_S \approx \frac{1}{g_m + g_{mb}} + R_D$$

$$\eta \approx \frac{g_{mb}}{g_m}$$



Apply to C.S. Ckt.

$$a_v = \frac{V_o}{V_i} = - \frac{g_m}{g_m + g_{mb}}$$

$$= - \frac{1}{(1+\eta)} \frac{g_{m1}}{g_{m2}} = a_v$$

$V_{gs1} \approx V_{gs2}$!

$$a_v = - \frac{1}{1+\eta} \frac{\sqrt{2\mu_n C_{ox}(W/L)_1 I_D}}{\sqrt{2\mu_p C_{ox}(W/L)_2 I_D}} = - \frac{1}{1+\eta} \sqrt{\frac{(W/L)_1}{(W/L)_2}} = a_v$$

We like μ ratio when doing this via wafer scale fab!

In IC's, it hard to achieve an absolute value, but it's easier to get an accurate ratios: $\frac{W_1}{W_2}$

Diode-Connected PMOS Load

$$a_v = - \frac{g_{m1}}{g_{m2}} = - \sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

PMOS Current Source Load

$$a_v = \frac{V_o}{V_i} = - g_m (r_{o1} || r_{o2})$$

$$= - \frac{g_{m1}}{g_{dri} + g_{dr2}}$$

$r_{o2} = \frac{1}{g_{dr2}}$

$r_{o1} = \frac{1}{g_{dri}}$

\Rightarrow gain is huge!
(because $r_o = \text{huge}$)

\neq but requires V_{BIAS}