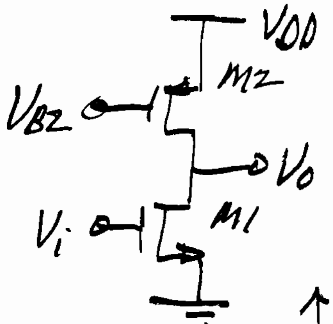
Today: High-Swing Current Mirrors (4.2.5.2 GM)

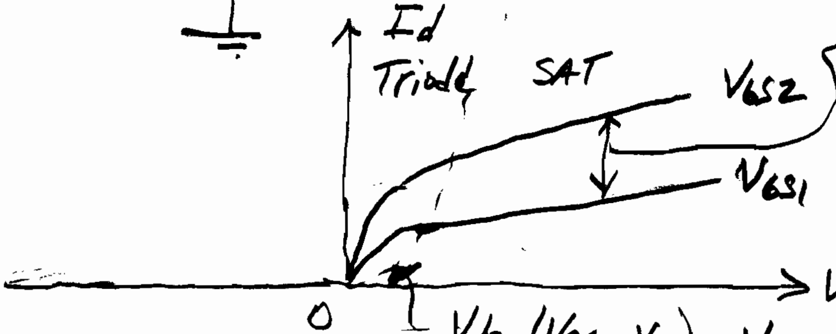
Motivation = High Dynamic Range (DR)

$$= \frac{V_{out}(max) \text{ — Limited by distortion}}{V_{out}(min) \text{ — Limited by noise}}$$

Let's consider output swing versus distortion:



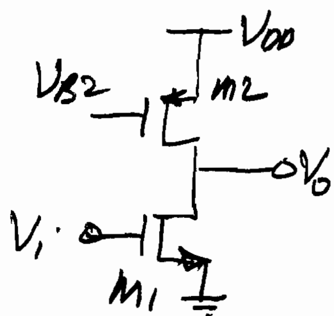

We know $a_v = -\frac{g_{m1}}{g_{o1}+g_{o2}}$ but this is only true with M1 and M2 in saturation. Why saturation?




$V_{ds} = (V_{gs} - V_T) = V_{OV}$

(1) $g_m = \frac{\Delta I}{\Delta V_{GS}}$ Bigger spacing in sat region means higher $g_m$.

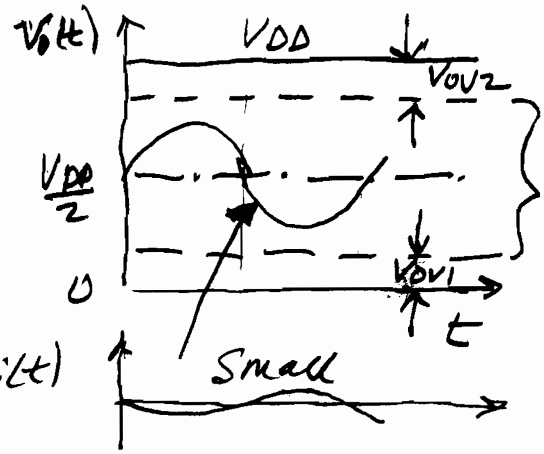
(2) $g_{o1}$ proportional to slope — small in sat but large in triode region




- M1 Saturation: $V_{DS1} \geq (V_{GS1} - V_{T1}) = V_{OV1}$
- M2 Saturation: $V_{SD2} \geq (V_{SG2} - |V_{T2}|) = V_{OV2}$

$V_{OV}$ values typically 100-200mV (100mV for VDD < ~1V)

So, with $V_o(DC) = V_{DD}/2$:

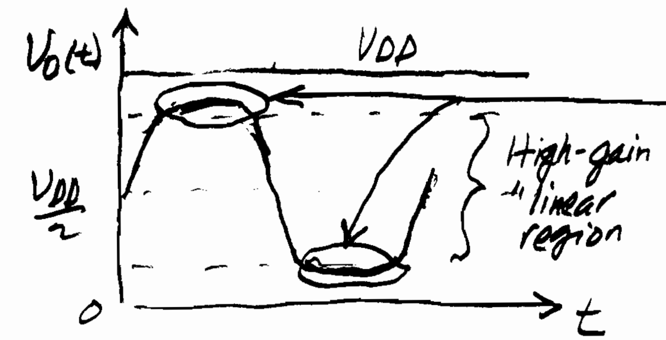



(i) High-gain linear region operation with a relatively small $V_i(t)$. Note:

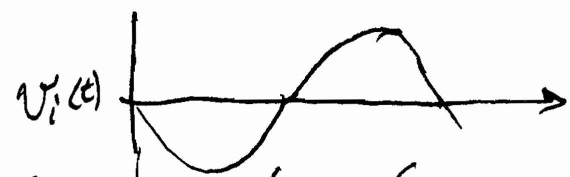
$V_{out}(min) > V_{OV1}$

$V_{out}(max) < V_{DD} - V_{OV2}$

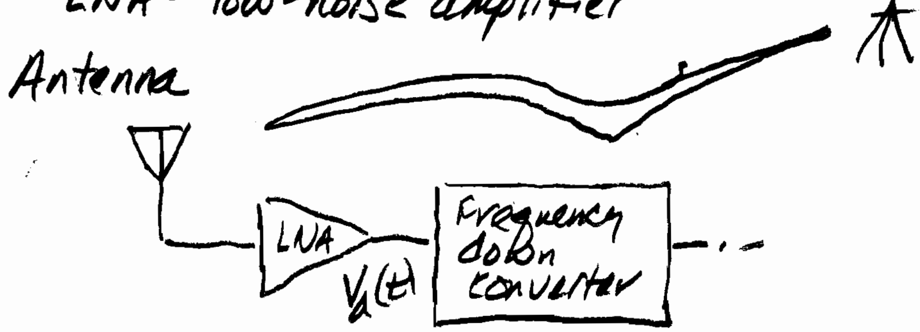
(ii) Relatively large input signal



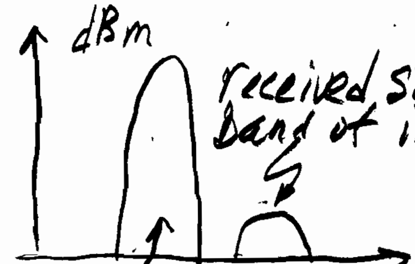

• low-gain nonlinear regions with high distortion levels.




• Example of performance degradation in this case — consider a cellphone receiver amplifier (i.e., an LNA - low-noise amplifier

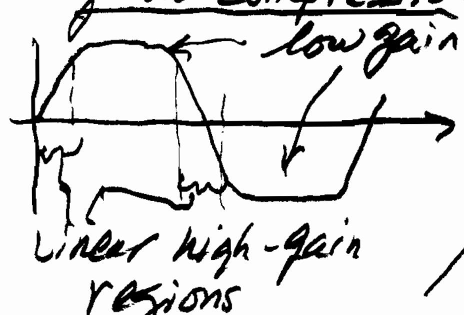



Transmitter may be far away.
∴ Very weak RF received signal.

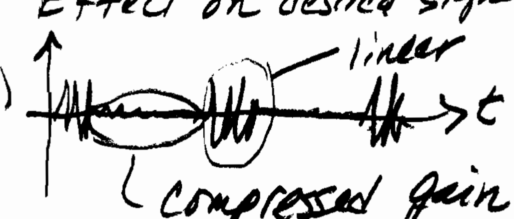



• LNA handles small signals linearly as in (i)

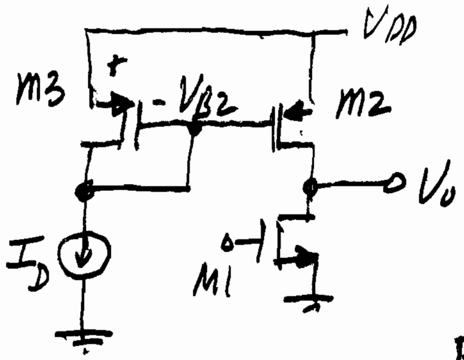
• Now, suppose a friend is nearby talk on his cellphone — Your phone will receive ~~this~~ signal too. Very large because close. What happens — Gain Desensitization or gain Compression due to blocker.




Effect on desired signal



- Simple current Mirror bias for CS Amp:



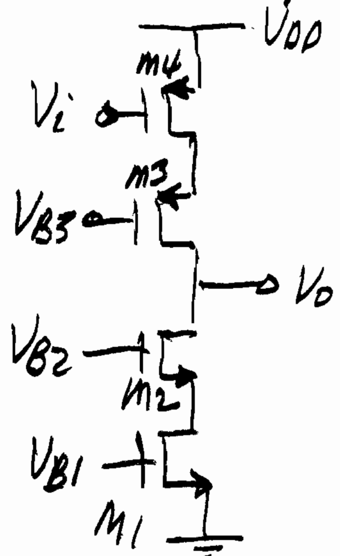

- Simple PMOS mirror generates $V_{B2}$:

$$V_{B2} = V_{DD} - V_{SG3}$$
$$= V_{DD} - |V_{T3}| - \underbrace{(V_{SG3} - |V_{T3}|)}_{V_{OV3}}$$

But, $V_{OV3} = \sqrt{\dfrac{2I_D}{k_p'(W/L)_3}}$

Thus, $V_o(\min) = V_{OV1}$ ; $V_o(\max) = V_{DD} - V_{OV2}$
$= V_{DD} - V_{OV3}$ } M2 and M3 are identical.

- Now, consider bias generators for a much better amplifier — cascode Amp




By inspection,

$$a_v \simeq - \frac{g_{m4}}{\dfrac{g_{o1}}{g_{m2} r_{o2}} + \dfrac{g_{o4}}{g_{m3} r_{o3}}}$$ (very large gain!)

Maintain M1-M4 in saturation over output voltage swing range.

- For the best possible design:

$V_{DS1} = V_{OV1}$ ; $V_{DS2}(\min) = V_{OV2}$
$V_{SD4} = V_{OV4}$ ; $V_{SD3}(\min) = V_{OV3}$ } Usually $V_{OVi} = V_{OV}$

Thus, $V_O(\max) = V_{DD} - V_{OV3} - V_{OV4} = V_{DD} - 2V_{OV}$

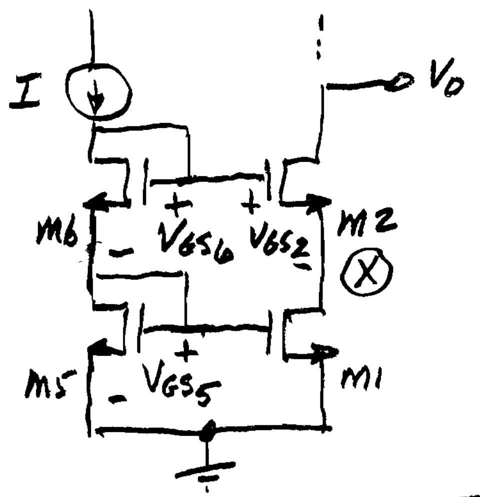
$V_O(\min) = V_{OV1} + V_{OV2} = 2V_{OV}$

$\therefore V_O(\text{swing}) = V_O(\max) - V_O(\min)$

$$= \boxed{V_{DD} - 4V_{OV}}$$

Example: $V_{DD} = 1.2\,V$, $V_{OV} = 100\,mV$ $\therefore V_O(\text{swing}) = \underline{\underline{0.8\,V}}$

Consider a cascode current source bias generator:




- $M_1$ & $M_5$ identical
- $M_2$ & $M_6$ indentical but not necessarily same as $M_1$, $M_5$

Find DC voltage $V_{\otimes}$:

$$V_{GS5} = V_{T5} + \sqrt{\frac{2I}{k_n'(W/L)_5}} = V_{T5} + V_{OV5} = V_{TNO} + V_{OV5}$$

$$V_{GS6} = V_{T6} + \sqrt{\frac{2I}{k_n'(W/L)_6}} = V_{T6} + V_{OV6} \quad (V_{T6} > V_{TNO})$$

$$V_{GS2} = V_{T2} + \sqrt{\frac{2I}{k_n'(W/L)_2}} = V_{T2} + V_{OV2} \quad (V_{T2} > V_{TNO})$$

KVL: $V_{\otimes} = V_{GS5} + V_{GS6} - V_{GS2}$ (Assume $V_{OV_i} = V_{OV}$)

$$= (V_{TNO} + V_{OV}) + (V_{T6} + V_{OV}) - (V_{T2} + V_{OV})$$

$$= V_{TNO} + V_{OV} + \underbrace{(V_{T6} - V_{T2})}_{=0} = \boxed{V_{TNO} + V_{OV}}$$

$\therefore$ $V_O(min) = V_{\otimes} + V_{OV2} = V_{TNO} + 2V_{OV}$

$V_O(max) = V_{DD} - |V_{TPO}| - 2V_{OV}$ (similar bias for $M_3$)

$\therefore$ $V_O(swing) = V_O(max) - V_O(min)$

$$= V_{DD} - \underbrace{(V_{TNO} + |V_{TPO}|)}_{\text{Very bad term for swing}} - 4V_{OV}$$

Example:

$V_{DD} = 1.2V$; $V_{TNO} = 0.5V$; $V_{TPO} = -0.5V$; $V_{OV} = 0.1V$

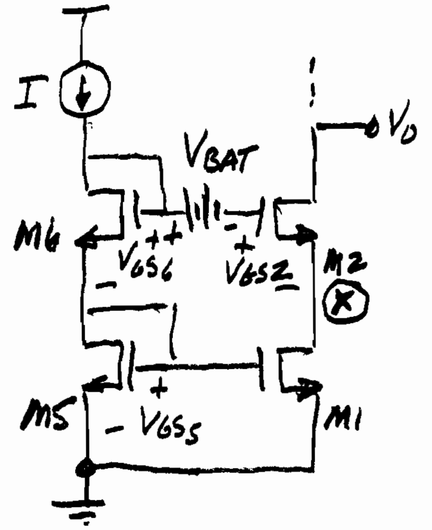
$V_O(swing) = 1.2 - (0.5 + 0.5) - 4(0.1) = \underline{-0.2V}$ !!

Not possible: Need $V_{DD} \geq 2V$ for $V_O(swing) \geq 0V$.

We want: $V_O(swing) = V_{DD} - 4V_{OV}$

$\therefore$ Get rid of two threshold voltage terms.

## Conceptual Solution: ~~Add~~ DC Level Shifter




KVL:

$V_{Ⓧ} = V_{GS5} + V_{GS6} - V_{BAT} - V_{GS2}$

$= V_{TNO} + (V_{T6} - V_{T2}) + V_{OV} - V_{BAT}$

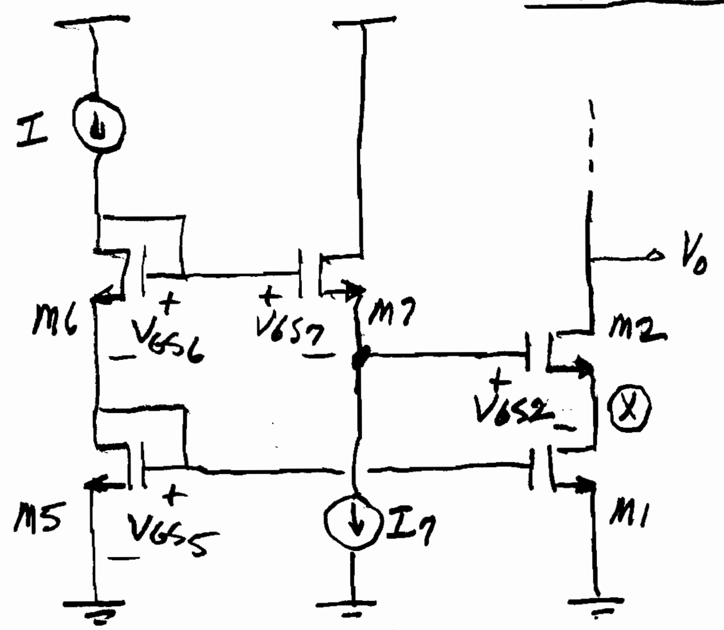
For $V_{Ⓧ} = V_{OV}$, we need:

$V_{BAT} = V_{TNO} + (V_{T6} - V_{T2})$

(Note: $V_{T6} > V_{T2}$ because $V_{SB6} = V_{GS5} = V_{TNO} + V_{OV}$ and $V_{SB2} = V_{OV}$) (Assume $V_{T6} = V_{T2}$)

$\therefore \boxed{V_{BAT} \simeq V_{TO}}$

Implement using NMOS source-follower:




KCL:

$V_{Ⓧ} = V_{GS5} + V_{GS6} - V_{GS7} - V_{GS2}$

Assuming $V_{Ti} = V_T$ and $V_{OVi} = V_{OV}$,

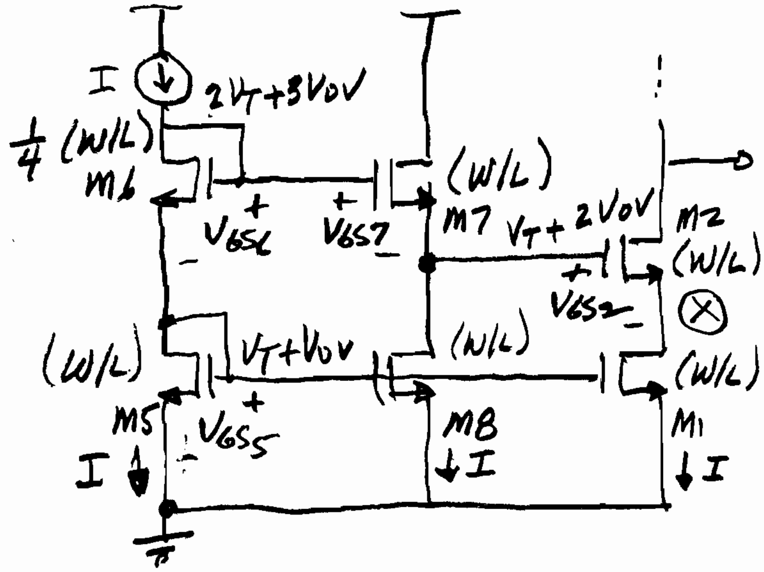
$V_{Ⓧ} = V_{OV}$ means $V_{OV7} \simeq 0$

$V_{OV7} = \sqrt{\dfrac{2I_7}{k_n'(W/L)_7}} \simeq 0$ means: i) $I_7 \simeq 0$ and/or ii) $(W/L)_7$ very big.

- Bad design because of weird way $M_7$ is used.
- Let's consider some sensible changes to this circuit based on our basic goals:

  (i) $V_{Ⓧ} = V_{OV}$

  (ii) $V_O(min) = 2V_{OV}$




- Assume all devices biased with $I$ as shown:

KVL: $V_{\otimes} = V_{GS5} + V_{GS6} - V_{GS7} - V_{GS2} = V_{ov}$

<u>Observation:</u> With $V_{Ti} = V_T$, $V_{\otimes}$ can only equal $V_{ov}$ if $V_{ov5}$ or $V_{ov6}$ equals $2V_{ov}$. Let's not mess with bottom row ($M5, M8, M1$) so lets design for $V_{ov6} = 2V_{ov}$ (i.e., $V_{ov1} = V_{ov2} = V_{ov5} = V_{ov7} = V_{ov8} = V_{ov}$)

$$V_{ov6} = \sqrt{\frac{2I}{k_n'(W/L)_6}} = 2V_{ov} \rightarrow \boxed{\left(\frac{W}{L}\right)_6 = \frac{1}{4}\left(\frac{W}{L}\right)_i \text{ for other devices}}$$

This is a practical size for $M_6$.

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<u>Body Effect Problem:</u> (All NMOS bulks to ground)

For $M_1, M_5, M_8$, $V_{SB} = 0$; $\therefore V_{T1} = V_{T5} = V_{T8} = V_{TN0}$

- But, $V_{SB} \neq 0$ for $M_2, M_7$ & $M6$:

$V_{SB6} = V_{S6} - \cancel{V_{B6}}^{0} = (V_{TN0} + V_{ov}) \rightarrow +\Delta V$ compared to $V_{TN0}$

$V_{SB7} = V_{S7} - \cancel{V_{B7}}^{0} = (V_{T2} + 2V_{ov}) \rightarrow ++\Delta V$ compared to $V_{TN0}$

$V_{SB2} = V_{S2} - \cancel{V_{B2}}^{0} = V_{ov} \rightarrow \Delta V$ compared to $V_{TN0}$

<u>Recall:</u> $V_{\otimes} = V_{GS5} + V_{GS6} - V_{GS7} - V_{GS2}$

$$= (V_{TN0} + V_{ov}) + (V_{T6} + 2V_{ov}) - (V_{T7} + V_{ov}) - (V_{T2} + V_{ov})$$

$$= \underbrace{(V_{TN0} - V_{T2})}_{<0} + \underbrace{(V_{T6} - V_{T7})}_{<0} + V_{ov}$$

$\boxed{\therefore V_{\otimes} < V_{ov}}$

Other problems with this circuit:

$V_{DS5} = V_{DS1}$ ∴ Current mismatch

$$I_1 = \frac{k_n'}{2}\left(\frac{W}{L}\right)_1 (V_{GS_1} - V_{TN0})^2 (1 + \lambda V_{DS1})$$

$$I_5 = \frac{k_n'}{2}\left(\frac{W}{L}\right)_5 (V_{GS_5} - V_{TN0})^2 (1 + \lambda V_{DS5}) = I_{REF} = I$$

$$\Rightarrow \frac{I_1}{I_5} = \frac{1 + \lambda V_{OV}}{1 + \lambda(V_{TN0} + V_{OV})} \simeq (1 + \lambda V_{OV})[1 - \lambda(V_{TN0} - V_{OV})]$$

$$\simeq 1 - \lambda(V_{TN0} - 2V_{OV})$$

- Would like $V_{DS5} = V_{DS1}$ for higher accuracy

Another issue is headroom requirement:

- At the drain of M6, $V_{D6} = 2V_T + 3V_{OV}$

Example: $V_{TN0} = 0.5V$; $V_{OV} = 0.1V$

$\Rightarrow V_{DD} > V_{D6} > 1.3V$

For modern CMOS processes: $V_{DD} = 1.2V$ or $V_{DD} = 0.8V$

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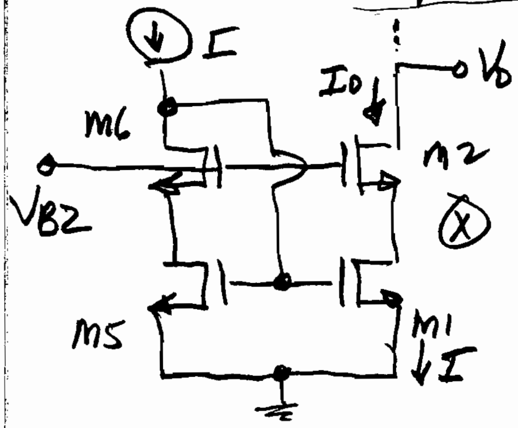
Solution: High-Swing Cascode Current Source




$V_{(X)} = V_{OV}$ (desired)

∴ $V_{B2} = V_T + 2V_{OV}$

Note: $V_{DS5} = V_{DS1} = V_{(X)} = V_{OV}$

∴ No systematic error in $I_{D1}$ versus $I_{D5}$.

But, $V_{D2} \neq V_{D6} = V_{GS_5}$.

This is usually not a problem because $I_O$ does not vary much from $I_{D1} = I_{D5} = I$ as set by $M_1$ and $M_5$. Why is this so?