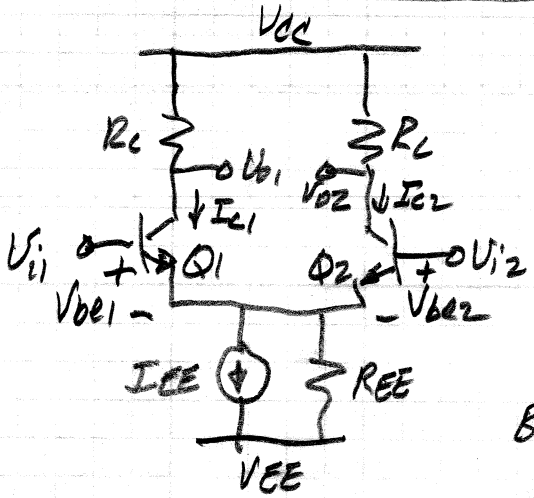
Large-Signal Performance of emitter-coupled pair:



KVL:

$$v_{i1} - v_{be1} + v_{be2} - v_{i2} = 0$$

$$v_{be1} = V_T \ln \frac{I_{C1}}{I_{S1}}; \quad v_{be2} = V_T \ln \frac{I_{C2}}{I_{S2}}$$

$$\therefore v_{i1} - v_{i2} - V_T \ln \frac{I_{C1}}{I_{C2}} = 0$$

But, $v_{id} = v_{i1} - v_{i2}$

$$\therefore v_{id} = V_T \ln \frac{I_{C1}}{I_{C2}} \quad \text{or} \quad \frac{I_{C1}}{I_{C2}} = e^{v_{id}/V_T} \qquad (1)$$

Neglect R_{EE}: $I_{EE} = I_{e1} + I_{e2}$

$$= \frac{I_{C1} + I_{C2}}{\alpha} \qquad (2)$$

$$\therefore \alpha I_{EE} = I_{C1} + I_{C2} = I_{C1} + I_{C1} e^{-v_{id}/V_T}$$

$$\Rightarrow I_{C1} = \frac{\alpha I_{EE}}{1 + e^{-v_{id}/V_T}} \quad \text{and} \quad I_{C2} = \frac{\alpha I_{EE}}{1 + e^{v_{id}/V_T}} \qquad (3)$$

Now, $v_{od} = v_{o1} - v_{o2} = (V_{CC} - I_{C1} R_C) - (V_{CC} - I_{C2} R_C)$

$$= (I_{C2} - I_{C1}) R_C$$

$$= \alpha I_{EE} R_C \left[\frac{1}{1 + e^{v_{id}/V_T}} - \frac{1}{1 + e^{-v_{id}/V_T}} \right]$$

Trick: multiply by: $\frac{e^{-v_{id}/2V_T}}{e^{-v_{id}/2V_T}}$ and $\frac{e^{v_{id}/2V_T}}{e^{v_{id}/2V_T}}$

$$= \alpha I_{EE} R_C \left[\frac{e^{-v_{id}/2V_T}}{e^{-v_{id}/2V_T} + e^{v_{id}/2V_T}} - \frac{e^{v_{id}/2V_T}}{e^{v_{id}/2V_T} + e^{-v_{id}/2V_T}} \right]$$

$$= \alpha I_{EE} R_C \left[\frac{e^{-v_{id}/2V_T} - e^{v_{id}/2V_T}}{e^{-v_{id}/2V_T} + e^{v_{id}/2V_T}} \right]$$

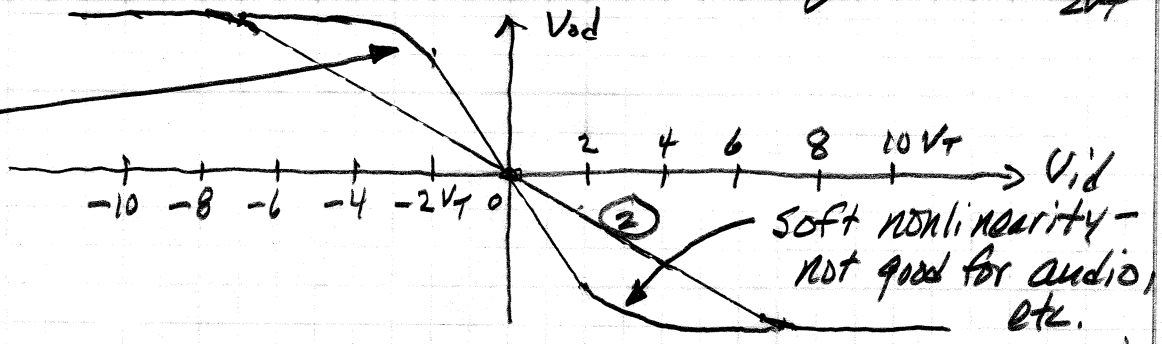
$$= \alpha I_{EE} R_C \frac{\sinh(-v_{id}/2V_T)}{\cosh(-v_{id}/2V_T)} = \boxed{\alpha I_{EE} R_C \tanh\left(\frac{-v_{id}}{2V_T}\right)}$$

note: $\sinh u = \frac{1}{2}(e^u - e^{-u})$; $\cosh u = \frac{1}{2}(e^u + e^{-u})$; $u = \frac{-v_{id}}{2V_T}$

$$V_{od} = \alpha I_{EE} R_C \tanh\left(\frac{-V_{id}}{2V_T}\right)$$

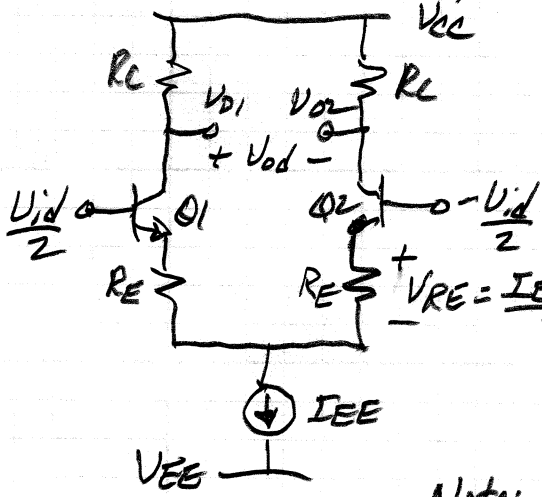
$$\simeq \alpha I_{EE} R_C \left[-\frac{V_{id}}{2V_T} + \frac{1}{3}\left(\frac{-V_{id}}{2V_T}\right)^3 - \frac{2}{15}\left(\frac{-V_{id}}{2V_T}\right)^5 + \cdots\right]$$

From Taylor series. Thus, V_{od} linear for small $\frac{V_{id}}{2V_T}$.

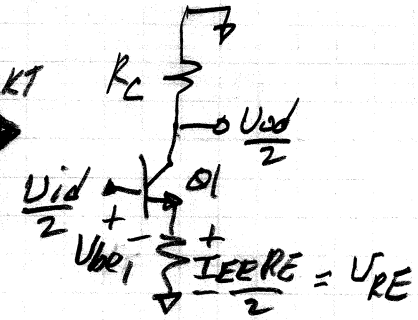


- Only linear for $-V_T < V_{id} < V_T$ (i.e., $|V_{id}| < 25\,mV$)

- Use emitter-degeneration to linearize the amp:



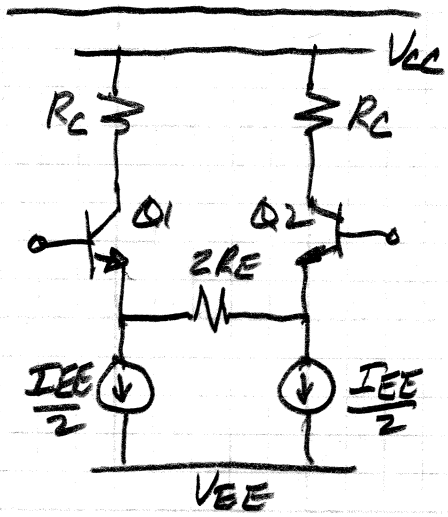
DM half-CKT



$$A_{dm} = \frac{-g_m R_C}{1 + g_m R_E} \simeq -\frac{R_C}{R_E} \quad \text{for } g_m R_E \gg 1 \text{ (curve 2)}$$

Note: $\frac{V_{id}}{2} = V_{be1} + V_{RE}$ $\left(g_m R_E = \frac{I_C R_E}{V_T} = \frac{V_{RE}}{V_T} \gg 1\right)$

$V_{be1} < V_T$ if V_{RE} is larger

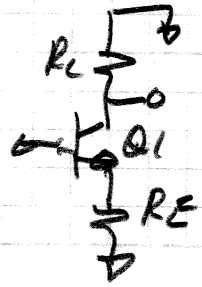


Low-Voltage Solution:

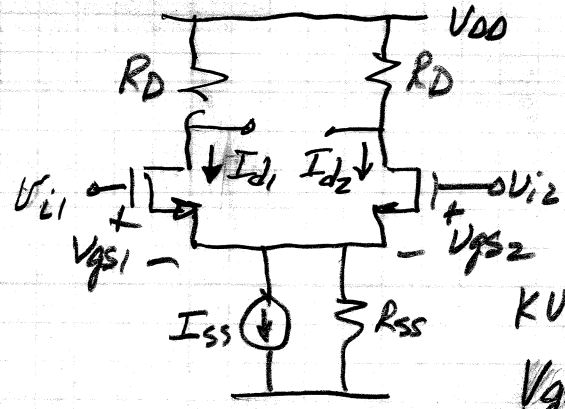
The solution above requires V_{RE} more headroom than this.

DM Half-circuit:

$$A_{dm} = \frac{-g_m R_C}{1 + g_m R_E}$$



Large-Signal Performance of NMOS source-coupled pair:



Assume: • M1 and M2 identical and operate in saturation
• neglect λ effects

• First, solve for $v_{id} = v_{i1} - v_{i2}$:

KVL: $v_{i1} - v_{gs1} + v_{gs2} - v_{i2} = 0$

$v_{gs1} = V_T + \sqrt{\frac{2I_{d1}}{k_n'(\frac{W}{L})}}$; $v_{gs2} = V_T + \sqrt{\frac{2I_{d2}}{k_n'(\frac{W}{L})}}$

$$\therefore\ v_{i1} - v_{i2} = v_{id} = \frac{\sqrt{I_{d1}} - \sqrt{I_{d2}}}{\sqrt{\frac{k_n'}{2}(\frac{W}{L})}} \quad (1)$$

But, KCL at common-source node (neglect R_{SS}):

$$I_{d1} + I_{d2} = I_{SS} \quad (2)$$

Thus, $$v_{id} = \frac{\sqrt{I_{d1}} - \sqrt{I_{SS} - I_{d1}}}{\sqrt{\frac{k'}{2}(\frac{W}{L})}} \quad (3)$$

Rearranging and using quadratic equation gives:

$$I_{d1} = \frac{I_{SS}}{2} \pm \frac{k'}{4}\left(\frac{W}{L}\right) v_{id} \sqrt{\frac{4I_{SS}}{k'(W/L)} - v_{id}^2}$$

But, $I_{d1} > \frac{I_{SS}}{2}$ when $v_{id} > 0$. Hence, only + solution is sensible. Thus,

$$\left.\begin{aligned} I_{d1} &= \frac{I_{SS}}{2} + \frac{k'}{4}\left(\frac{W}{L}\right) v_{id} \sqrt{\frac{4I_{SS}}{k'(W/L)} - v_{id}^2} \\ \text{and } I_{d2} &= \frac{I_{SS}}{2} - \frac{k'}{4}\left(\frac{W}{L}\right) v_{id} \sqrt{\frac{4I_{SS}}{k'(W/L)} - v_{id}^2} \end{aligned}\right\}$$

• No triode operation by assumption so limitation on v_{id} is cutoff region of operation:

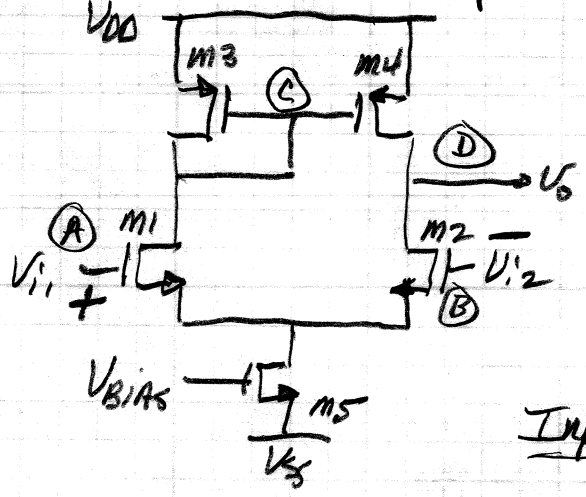
M1 off when $I_{d2} = I_{SS}$: (1) → $|v_{id}| \le \sqrt{\frac{2I_{SS}}{k'(W/L)}}$

$I_{d1} = \frac{I_{SS}}{2}$ when $v_{id} = 0$

→ $|v_{id}| \le \sqrt{2}\, V_{OV}$

Designer control w/o R_S degeneration!

• MOS Differential pair with current mirror load:



Question: polarity of inputs?

- Count number of inversions from input(s) to output(s):

Note: Common-source stage is only basic inverting stage.

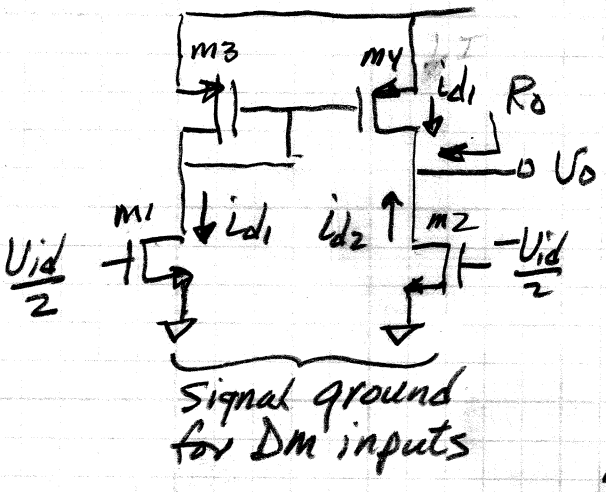
Input V_{i1}: $\frac{V_C}{V_A}$ & $\frac{V_D}{V_C}$ inverting.

Even number = 2 ∴ V_{i1} is (+) input

Input V_{i2}: $\frac{V_D}{V_B}$ is inverting. Odd number = 1

∴ V_{i2} is (−) input

How does this stage operate? Consider DM inputs:



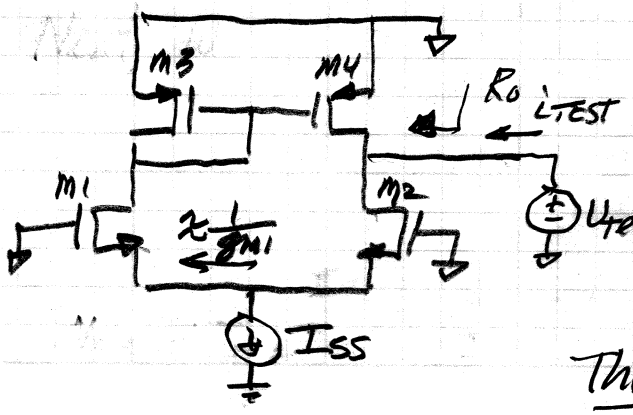
$i_{d1} = g_{m1}\frac{V_{id}}{2} = g_m\frac{V_{id}}{2}$

$i_{d2} = g_m\frac{V_{id}}{2}$ (note: current direction opposite for negative sign)

But, m3-m4 mirror i_{d1} into V_o node as shown.

∴ $V_o = (i_{d1} + i_{d2})R_o$

∴ Full DM gain is realized! $= g_m R_o V_{id}$ ∴ $\boxed{A_{dm} = g_m R_o}$



- Find R_o by inspection:

$R_o = R_{o\uparrow} // R_{o\downarrow}$

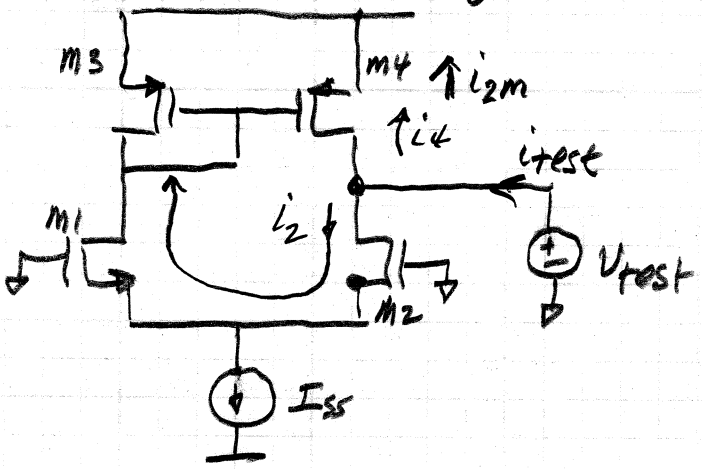
$R_{o\uparrow} = r_{o4}$

$R_{o\downarrow} \simeq r_{o2}\left(1 + \frac{g_{m2}}{g_{m1}}\right) \simeq 2r_{o2}$

This is wrong! Why?

- There is feedback in this circuit. Inspection method usually fails when there is feedback

- Let's find R_o using feedback:



$i_4 = \frac{V_{test}}{r_{O4}}$

$i_2 \simeq \frac{V_{test}}{2r_{O2}}$

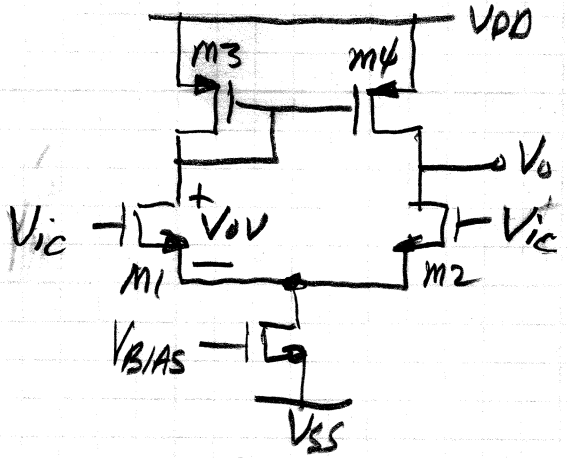
But, i_2 is mirrored to the output node as shown. $i_{2m} \simeq i_2 = \frac{V_{test}}{2r_{O2}}$

$\therefore i_{test} = V_{test}\left(\frac{1}{r_{O4}} + \frac{1}{2r_{O2}} + \frac{1}{2r_{O2}}\right) = V_{test}\left(\frac{1}{r_{O4}} + \frac{1}{r_{O2}}\right)$

$\therefore \boxed{G_{out} = g_{O2} + g_{O4}}$

correct answer but understand where it came from.

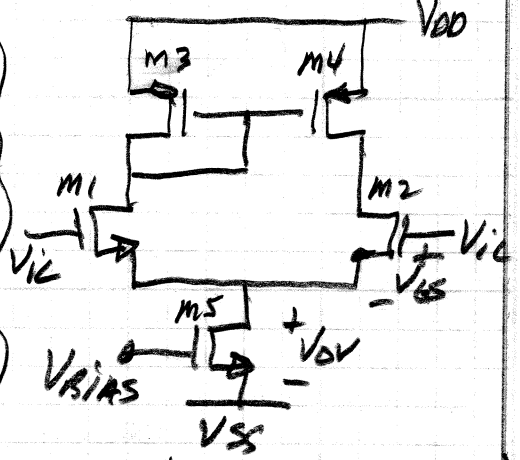
- Common-mode Performance:



$V_{ic}(max) = CMR^+$ (M1 triode):

$V_{DD} - V_{SG3} - V_{OV1} + V_{GS1} = V_{ic}(max)$

$\boxed{V_{ic}(max) = V_{DD} - V_{OV}}$ (Equal $|V_t|$ and equal V_{OV})

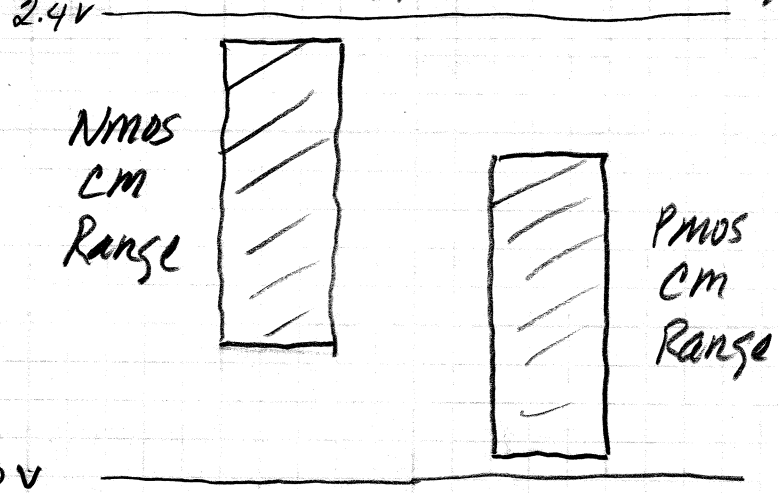


$V_{ic}(min) = CMR^-$ (M5 triode):

$V_{ic}(min) - V_{GS1} - V_{OV} - V_{SS} = 0$

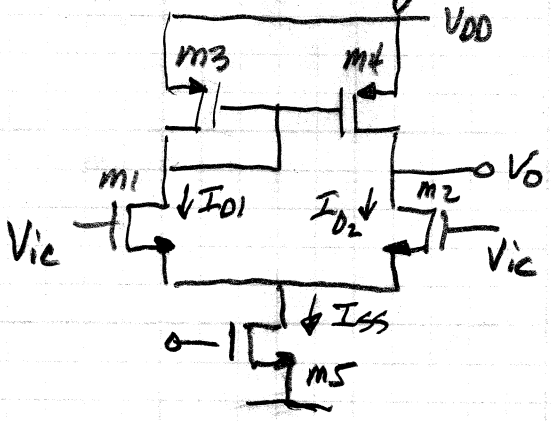
$\boxed{V_{ic}(min) = V_{SS} + V_T + 2V_{OV}}$

Note: NMOS pair CMR^+ close to V_{DD} (e.g., $V_{DD}-0.1V$) but CMR^- not close to V_{SS} (e.g., $V_{SS}+0.7V$)
PMOS pair has opposite CM Range performance.



- When full CM Range is required, use PMOS and NMOS pairs in parallel. Tricky designs!

Common-mode gain analysis:



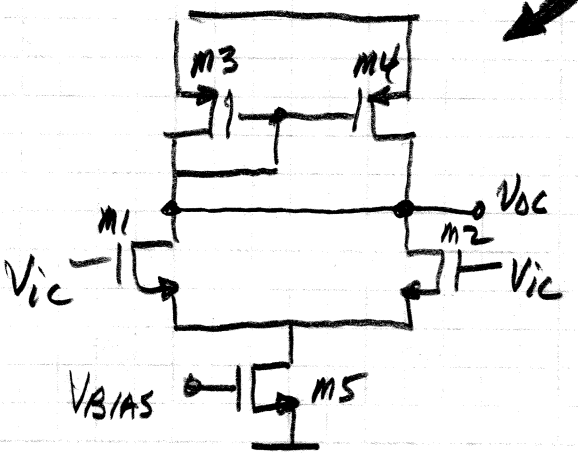
- Assume matched pairs

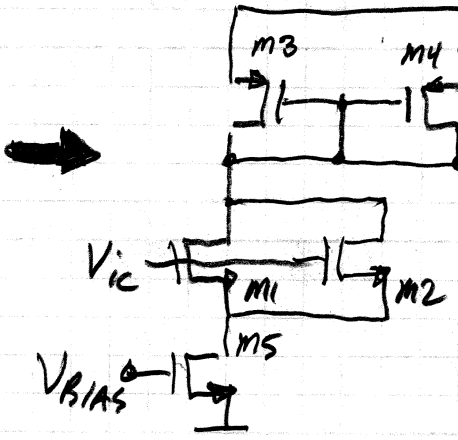
$\therefore I_{D1} = I_{D2} = I_{SS}/2$

Key observation:

$I_{D1} = I_{D2} \therefore V_{SD_3} = V_{SD4}$

Thus, we can analyze by shorting as shown below:





This is just a degenerated CS Amp.

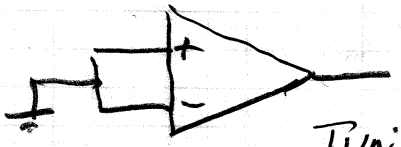
By inspection: (neglect $R_{O\downarrow}$ which is large compared to diode-connected M3 and M4:

$$G_m = \frac{g_{m1}+g_{m2}}{1+(g_{m1}+g_{m2})r_{O5}} = \frac{2g_{m1}}{1+2g_{m1}r_{O5}}$$

$$A_{CM} = G_m R_O \simeq \frac{2g_{m1}}{1+2g_{m1}r_{O5}} \cdot \frac{1}{g_{m3}+g_{O3}+g_{m4}+g_{O4}}$$

$$\simeq \frac{2}{1+2g_{m1}r_{O5}} \simeq \frac{1}{g_{m1}r_{O5}} \quad \left(\text{For } g_{m1}=g_{m3},\ 2g_{m1}r_{O5} \gg 1, \text{ etc}\right)$$

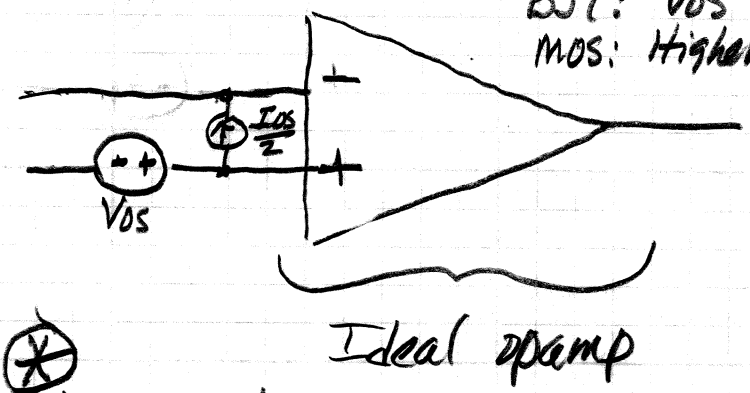
- Input offset Voltage
- Pairs of devices are mismatched due to process variations as we saw before with capacitors: Effect – outputs railed in open loop



$V_O = A_{dm}(v^+ - v^-) \rightarrow V_{DD}$ or V_{SS} with V_{OS}

Typical Values: V_{OS} few mV.

How to model – input-referred so as to be able to compare to the size of the input signal.



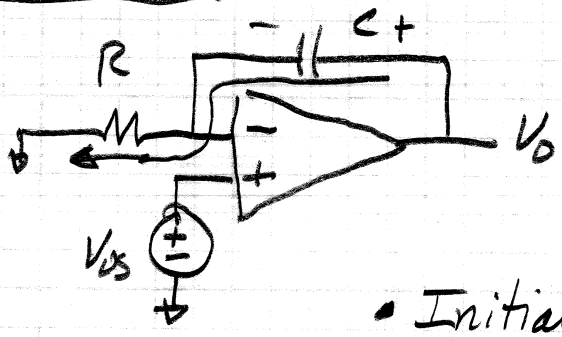
BJT: V_{OS} 1-5 mV
MOS: Higher

In BJT:
$I_{OS} = I_{B1} - I_{B2}$
In MOS:
$I_{OS} = 0$

Ideal opamp

V_{OS} = Voltage needed in the configuration above to set $V_O = 0$ (or $V_{DD}/2$ as appropriate)

Vos Problems: consider Miller Integrator



negative Feedback.

$\therefore V^- = V^+ = V_{os}$

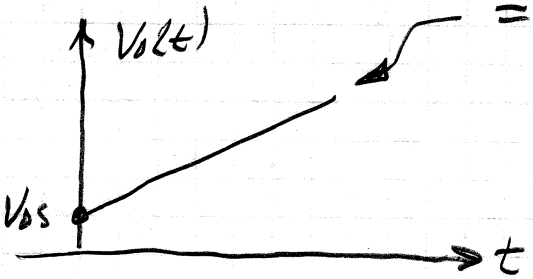
$I = \frac{V_{os}}{R}$

- Initial condition: Assume $V_c = 0$

$\therefore V_o = V_{os}$

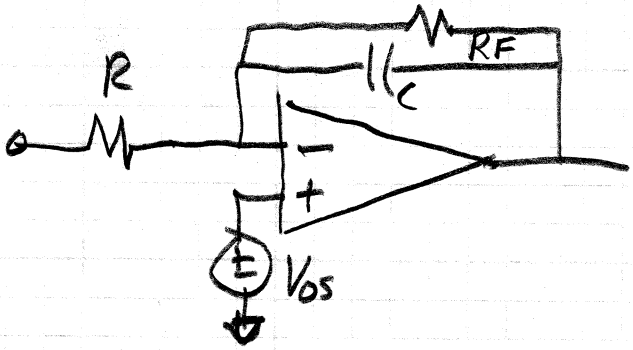
$$V_o = V_{os} + \frac{1}{C}\int_0^t I\,dt = V_{os} + \frac{V_{os}}{RC}t$$

$$= V_{os}\left(1 + \frac{t}{RC}\right)$$



V_o will rail at V_{DD} over time.

One solution: (Add feedback resistor)



$$V_o = V_{os}\left(1 + \frac{R_F}{R}\right)$$

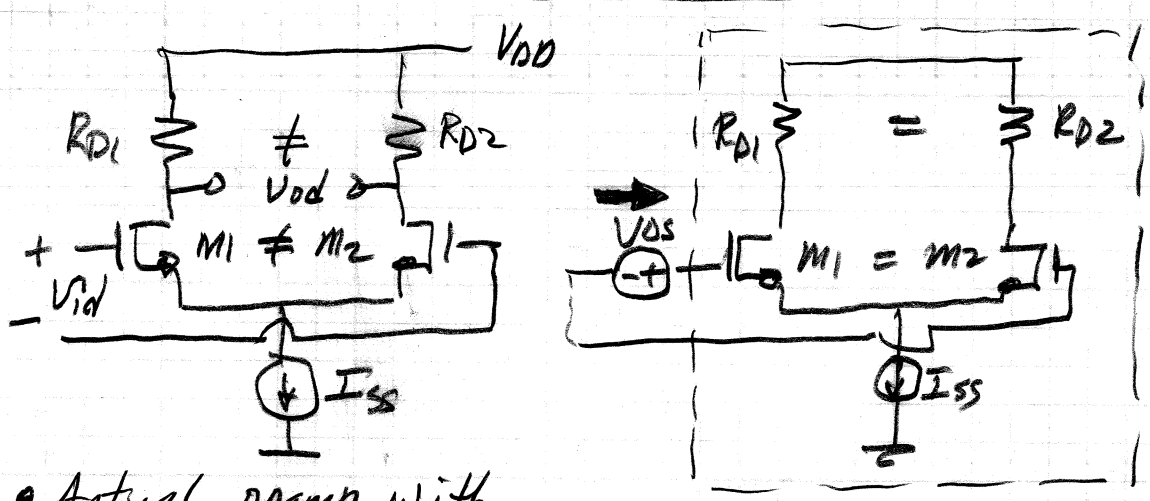
So output does not rail due to V_{os}.

But, R_F large so that C dominates (i.e., integrator)

So large DC offset at output.

- Precision circuits use offset cancellation techniques.

V_{OS} of mismatched NMOS Differential Pair:



- Actual opamp with device mismatches
- Ideal ≡ no mismatches
  But input equivalent V_{OS}

V_{OS} arises due to mismatches in devices:

- $M1 \neq M2$ — (W/L) and V_t variations
  (neglect k' and λ variations)
- R_{D1} and R_{D2} mismatches

- Definition: $V_{id} = V_{OS}$ causes $V_{od} = 0$

KVL: $V_{OS} - V_{GS1} + V_{GS2} = 0$

$$V_{OS} = \left(V_{t1} + \sqrt{\frac{2I_{D1}}{k'(W/L)_1}}\right) - \left(V_{t2} + \sqrt{\frac{2I_{D2}}{k'(W/L)_2}}\right)$$

$$= (V_{t1} - V_{t2}) + \left(\sqrt{\frac{2I_{D1}}{k'(W/L)_1}} - \sqrt{\frac{2I_{D2}}{k'(W/L)_2}}\right) \quad (1)$$

- Define average and difference quantities as before:

$$= \Delta V_t + \sqrt{\frac{2\left(I_D + \frac{\Delta I_D}{2}\right)}{k'\left[(W/L) + \frac{\Delta(W/L)}{2}\right]}} - \sqrt{\frac{2\left(I_D - \frac{\Delta I_D}{2}\right)}{k'\left[(W/L) - \frac{\Delta(W/L)}{2}\right]}}$$

Also use $V_{od} = 0$

$$\rightarrow I_{D1} R_{D1} = I_{D2} R_{D2} \quad \therefore \quad \frac{\Delta I_D}{I_D} = -\frac{\Delta R_D}{R_D}$$

$$V_{OS} = \Delta V_t + \frac{1}{2}(V_{GS} - V_t)\left\{-\frac{\Delta R_D}{R_D} - \frac{\Delta(W/L)}{(W/L)}\right\}$$