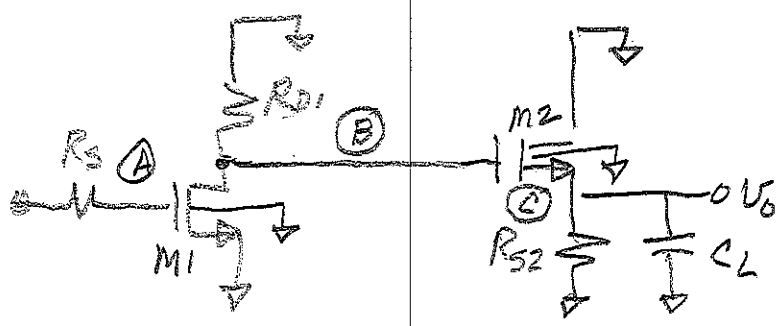
• Dominent Pole Estimation by inspection:



Two-stage Example:
• Cascade of CS and CD stages

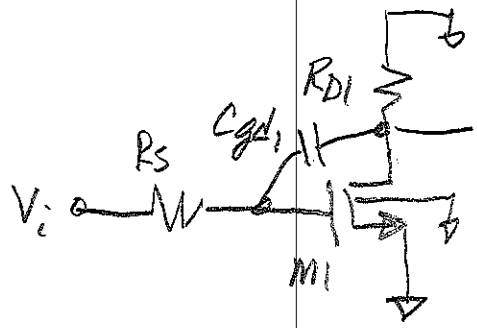
i) Short large coupling and bypass caps (none):

ii) Identify all contributing transistor caps

M1: C_{gd1} — yes (A) & (B)
C_{gs1} — yes (A)
C_{gb1} — yes (A)
C_{db1} — yes (B)
C_{sb1} — No, shorted

M2: C_{gd2} — yes (B)
C_{gs2} — yes (B) & (C)
C_{gb2} — yes (B)
C_{db2} — No, shorted
C_{sb2} — yes (C)

iii) Identify total capacitance to ground at (A):

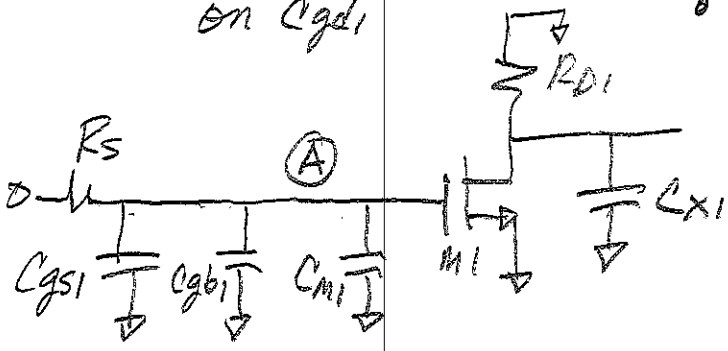


Miller Effect:

$$C_{M1} = C_{gd1}(1 - A_{vo}) = C_{gd1}\left(1 + \frac{g_{m1}}{g_{ds1} + g_{D1}}\right)$$

$$C_X = C_{gd1}\left(1 - \frac{1}{A_{vo}}\right) \simeq C_{gd1}$$

Miller Effect on C_{gd1}



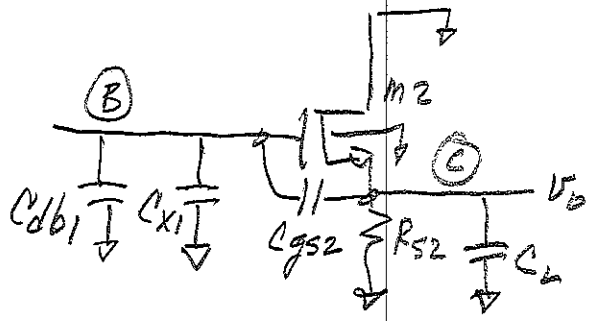
• Driving Point Resistance

Replace $(C_{gs1} + C_{gb1} + C_{M1})$ by Vtest. By Inspection,

$R_A = R_S$

$$\therefore \boxed{\tau_A = R_S(C_{gs1} + C_{gb1} + C_{M1})}$$

• Now, move to (B) but Miller Effect on C_{gs2}:



Miller Effect:

$$C_{M2} = C_{gs2}(1 - A_{vo})$$

$$= C_{gs2}\left(1 - \frac{g_{m2}}{g_{m2} + g_{mbs2} + g_{ds2} + g_{s2}}\right)$$

$$= C_{gs2}\left(\frac{g_{mbs2} + g_{ds2} + g_{s2}}{g_{m2} + g_{mbs2} + g_{ds2} + g_{s2}}\right)$$

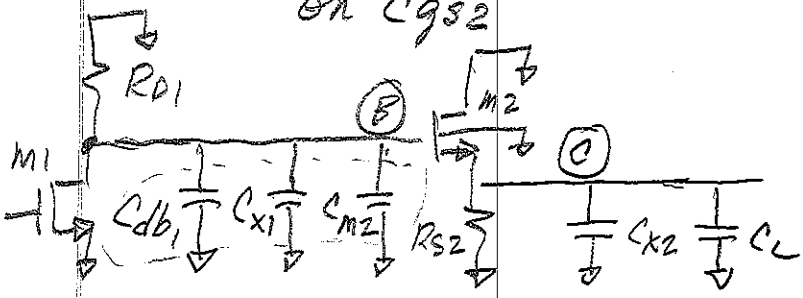
• C_{gs2} is bootstrapped so its effect at (B) is reduced.

$$C_{X2} = C_{gs2}\left(1 - \frac{1}{A_{vo}}\right)$$

$$= -C_{gs2}\left(\frac{g_{mb2} + g_{ds2} + g_{s2}}{g_m}\right)$$

• Negative capacitance added at (C), (Replace parallel caps with V_{test})

Miller Effect on C_{gs2}



Driving point resistance at (B):

$$R_B = R_{D1} \,//\, r_{ds1} = \frac{1}{g_{D1} + g_{ds1}}$$

$$\therefore \boxed{\tau_B = \frac{C_{db1} + C_{x1} + C_{M2}}{g_{d1} + g_{ds1}}}$$

Driving point resistance at (C): (By inspection)

$$R_C = \frac{1}{g_{m2} + g_{mb2} + g_{ds2} + g_{s2}}$$

(Replace parallel caps with V_{test})

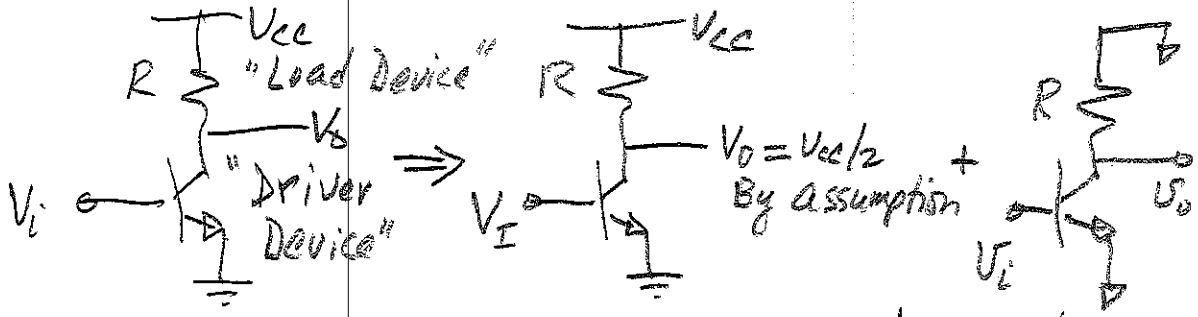
$$\therefore \boxed{\tau_C = \frac{C_{X2} + C_L}{g_{m2} + g_{mb2} + g_{ds2} + g_{s2}}}$$

• Dominant pole $\Rightarrow$ $\omega_{-3dB} = \frac{1}{b_1} = \frac{1}{\sum \tau_i} = \frac{1}{\tau_A + \tau_B + \tau_C}$

- Let's move on to active loads:

Motivations: 1) Passive R loads are costly in terms of chip area
2) Passive R loads are a fundamental limit to achievable gain.

- Consider a simple CE stage with R load:



$I_C = \frac{V_{CC}}{2R}$

(neglect r_o; i.e., assume $V_A \to \infty$)

$$A_v = -g_m R = -\frac{I_C}{V_T} R = \boxed{-\frac{V_{DD}}{2V_T}}$$

Gain limited by V_{DD}.

Example: $V_{DD} = 5$ V; $A_v = \frac{-5}{50\,mV} = \boxed{-100\ V/V}$

- Also, as time marches on, V_{DD} is generally being reduced due to scaling effects

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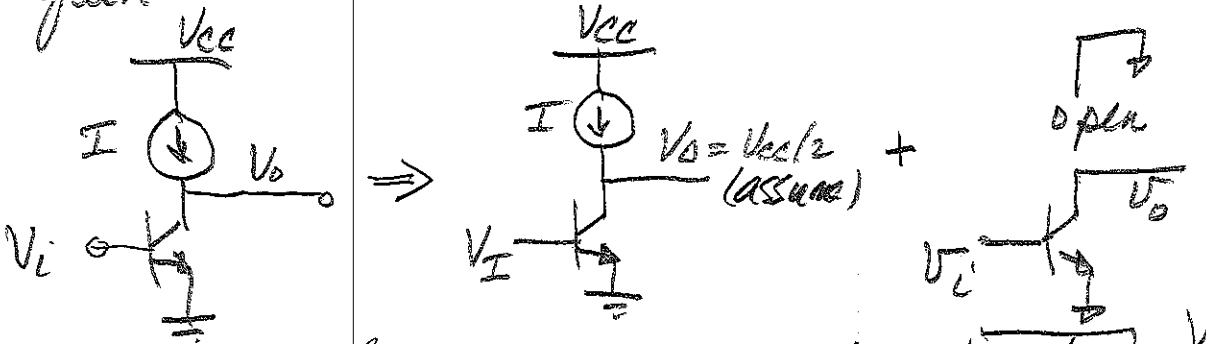
Recall best-case gain = open-circuit voltage gain

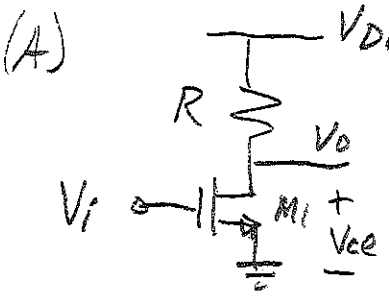


$$\text{so } A_v = -g_m r_o = -\frac{I}{V_T} \cdot \frac{V_A}{V_T} = \boxed{-\frac{V_A}{V_T}} \qquad V_A \gg V_{CC}$$

The purpose of an active load is to approximate as closely as possible an ideal current source.
Typical Limitations: i) Norton resistance < ∞
ii) Output voltage swing limits.

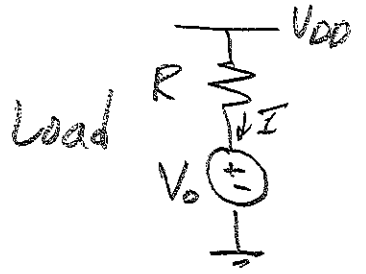
Consider several types: (MOS CS Stages)

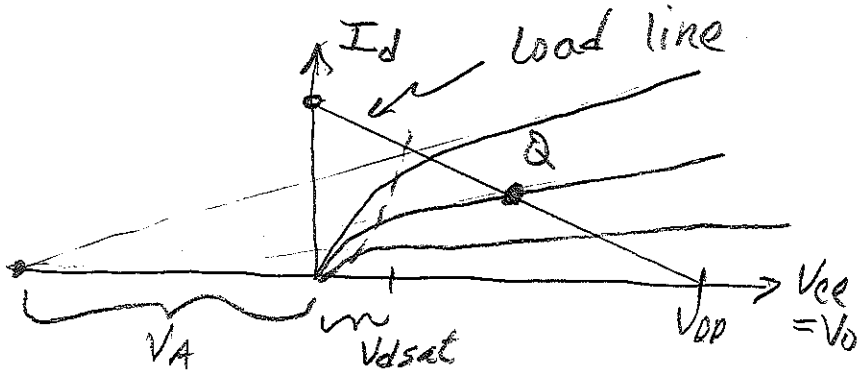
(A)



$$a_v = -\frac{g_m}{g_{ds}+g}$$ (For M1 in Saturation)

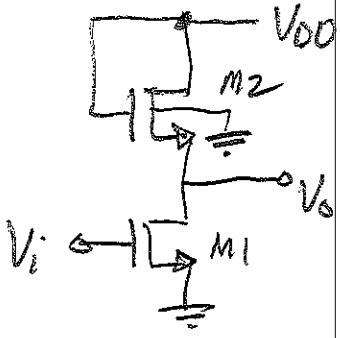
Recall: Load-line Construction





⇒ Large area (cost) and low gain but maximum V_o swing from $V_{dsat} = (V_{GS} - V_t)$ to V_{DD}.

(B) NMOS "diode" load:



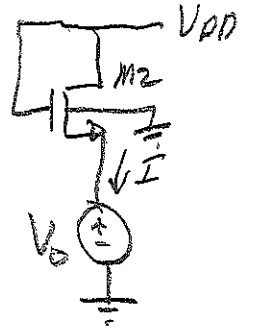
By inspection:

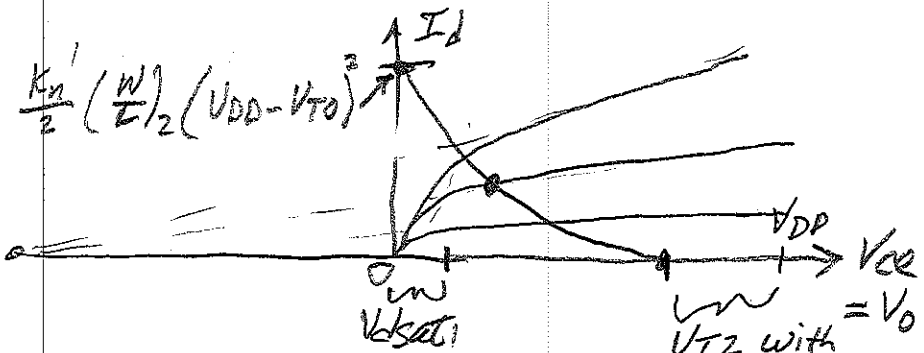
$$a_v = -\frac{g_{m1}}{g_{m2}+g_{mb2}+g_{ds2}+g_{ds1}}$$

$$\simeq -\frac{g_{m1}}{g_{m2}}\frac{1}{(1+\eta)}$$

$$\simeq -\frac{\sqrt{(W/L)_1}}{\sqrt{(W/L)_2}}\frac{1}{(1+\eta)}$$

low-gain but well controlled because of (W/L) ratio.

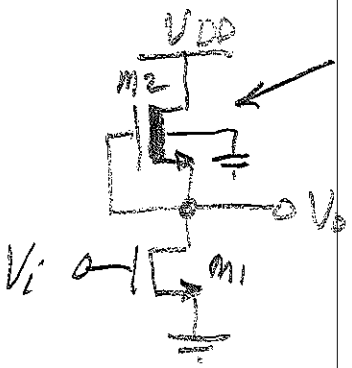




Output Voltage Swing: $V_o(max) = V_{DD} - V_{T2}$

$V_o(min) = V_{dsat_1} = (V_{GS} - V_{TO})_1$

(c) NMOS Depletion load:



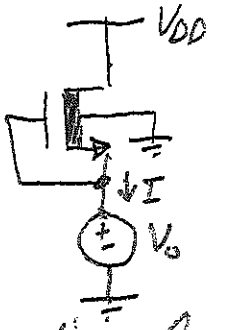
Depletion device $\Rightarrow V_{TO2} < 0$ (typically -3 V in old days)

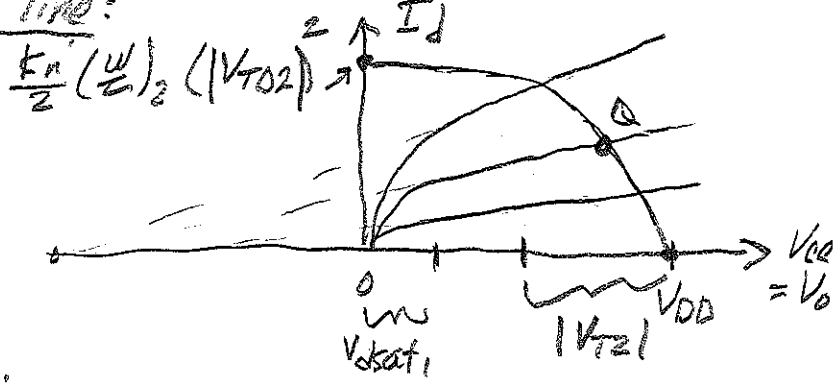
Idea: Approximate constant current source - $I_{D2} = \frac{K_n'}{2}\left(\frac{W}{L}\right)_2 (|V_{T2}|)^2$ with $V_{GS2} = 0$

Again, by inspection:

$$A_v = -\frac{g_{m1}}{g_{mb2} + g_{ds2} + g_{ds1}} \simeq -\frac{g_{m1}}{g_{mb2}}$$

Now consider load line:





Saturation for M2:

$V_{DS} \geq V_{GS} - |V_{T2}| \Rightarrow V_o \leq V_{DD} - |V_{T2}|$

$\therefore$ Hence, $V_o(max) = V_{DD} - |V_{T2}|$

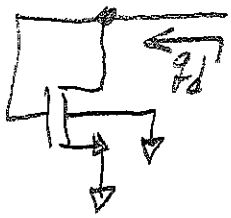
$V_o(min) = V_{dsat_1}$

Perhaps 3x more gain than diode load but limited output voltage swing range (Poor linearity)

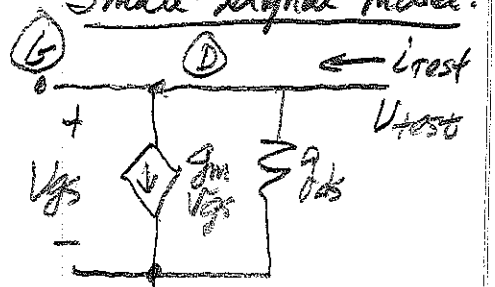
Consider NMOS diode-connected device:

$g_s = g_m + g_{mb} + g_{ds}$

"Diode" is not symmetric

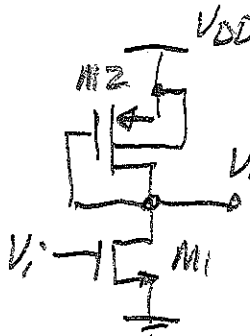


Small-signal model:



$$\Rightarrow \boxed{g_d = g_m + g_{ds}}$$

(D) PMOS diode load:



Based on the analysis above:

$$A_v = \frac{-g_{m1}}{g_{m2} + g_{ds2} + g_{ds1}}$$

$$\simeq -\frac{g_{m1}}{g_{m2}}$$

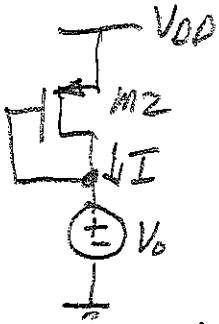
$$= -\frac{\sqrt{2k_n'(W/L)_1 I_D}}{\sqrt{2k_p'(W/L)_2 I_D}}$$

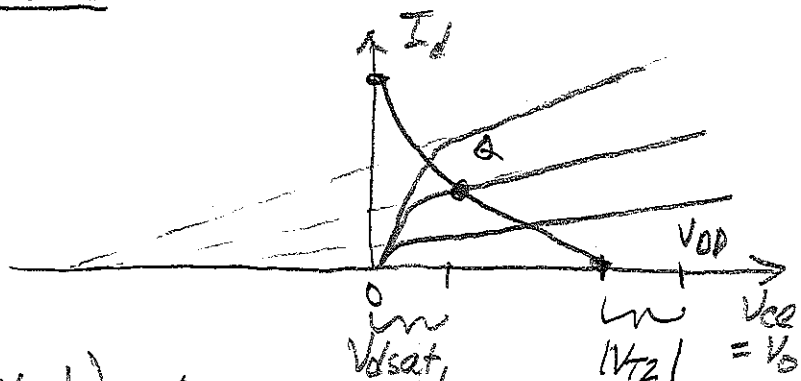
$$= -\sqrt{\frac{k_n'}{k_p'}\left(\frac{W_1}{W_2}\right)\left(\frac{L_2}{L_1}\right)}$$

$\frac{k_n'}{k_p'}$: k_p ratio usually $\simeq 2$-3

Note: Diode connected device operates in two regions only: cutoff or saturation

Now, consider load line:



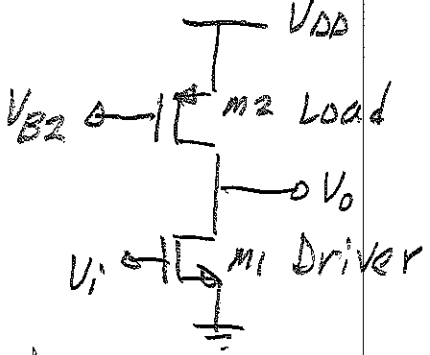


M2 cutoff: $(V_{sg} - |V_{T2}|) = 0$

$V_{sg} = |V_{T2}| = V_{DD} - V_{o(max)} \Rightarrow V_{o(max)} = V_{DD} - |V_{T2}|$

$V_{o(min)} = V_{dsat,1}$

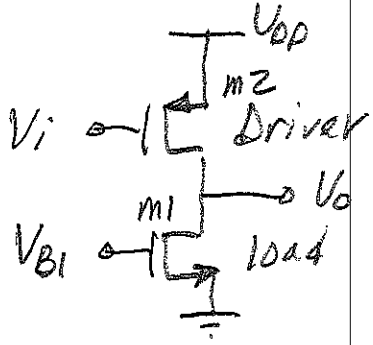
(E) PMOS Current source load:



By inspection:

$$A_v = -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$ (very high gain)

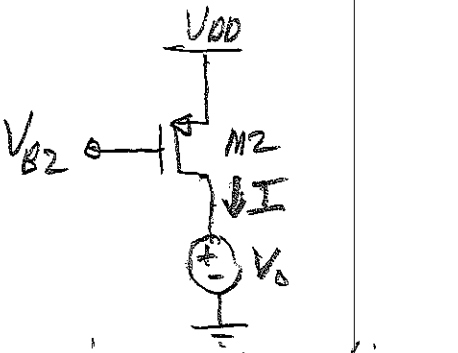
(F) NMOS Current source load:

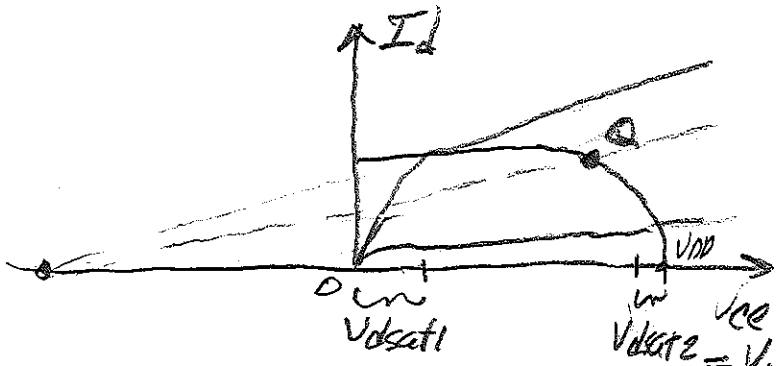


By inspection:

$$A_v = -\frac{g_{m2}}{g_{ds1} + g_{ds2}}$$ (Slightly less gain than above for same I because $k_p' < k_n'$)

Back to PMOS Current Source load line:





M2 in Saturation:

$V_{SD2} \geq (V_{SG2} - |V_{T2}|)$

$(V_{DD} - V_o) \geq (V_{DD} - V_{B2} - |V_{T2}|)$

$\Rightarrow V_o \leq V_{B2} + |V_{T2}|$

$\therefore V_{o(max)} = V_{DD} - V_{DSAT2}$

$V_{o(min)} = V_{dsat1}$

$\therefore$ highest gain and output swing range

Example: $V_{DD} = 5V$

$V_{T2} = -0.5V$

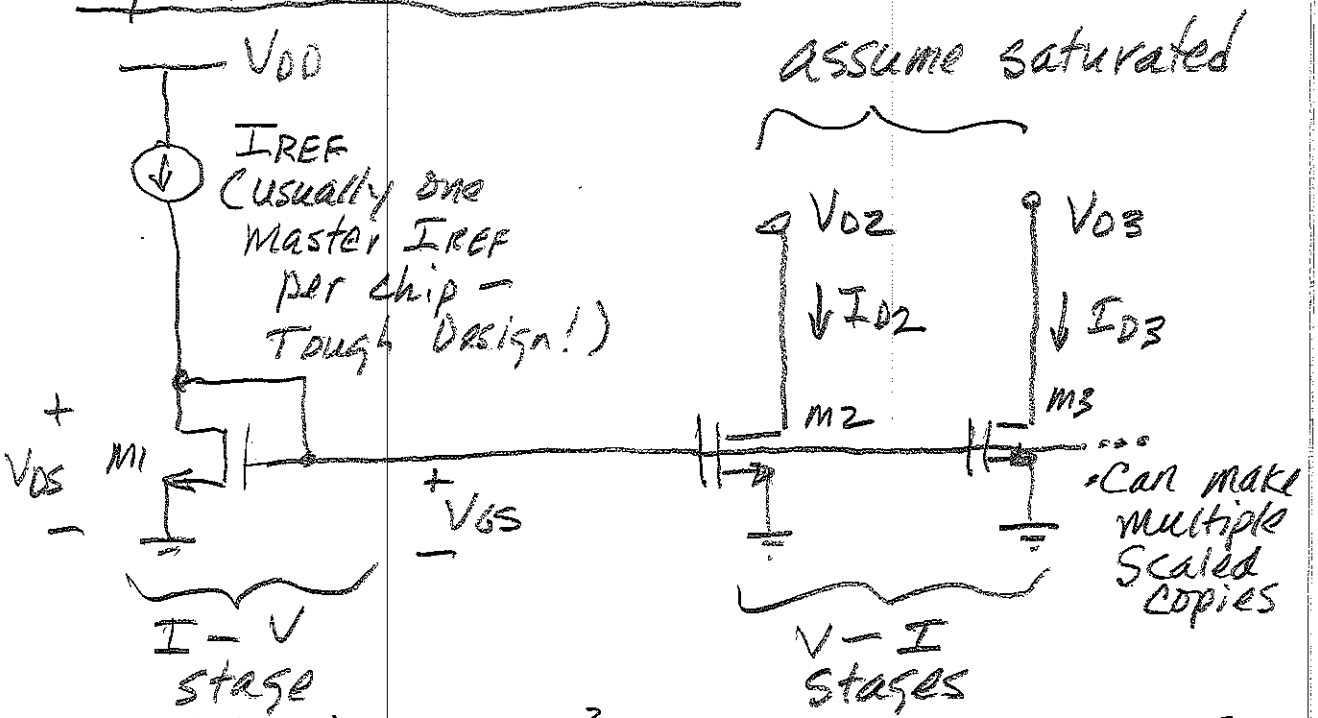
$V_{B2} = 4.3V$

$V_{o(max)} = V_{B2} + |V_{T2}|$

$= 4.3V + 0.5V$

$= 4.8V$

Simple NMOS Current Source:



$$I_{REF} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_1 (V_{GS}-V_T)^2 \Rightarrow V_{GS} = V_T + \sqrt{\frac{2I_{REF}}{k_n'(W/L)_1}}$$

$$\therefore I_2 = \frac{k_n'}{2}\left(\frac{W}{L}\right)_2 (V_{GS}-V_T)^2$$

$$= \frac{k_n'}{2}\left(\frac{W}{L}\right)_2 \left[\left(V_T + \sqrt{\frac{2I_{REF}}{k_n'(W/L)_1}}\right) - V_T\right]^2$$

$$= \frac{k_n'}{2}\left(\frac{W}{L}\right)_2 \left[\frac{2I_{REF}}{k_n'(W/L)_1}\right]$$

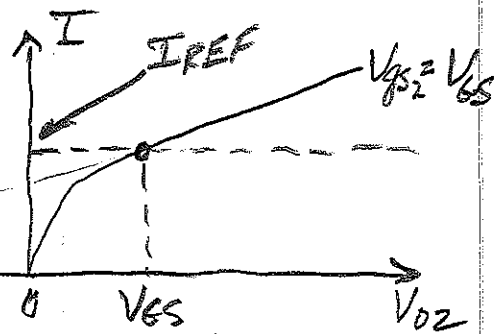
$$= \frac{(W/L)_2}{(W/L)_1} I_{REF} \longleftarrow I_2$$

Note: Usually use same L's for all related current source devices.

How accurate?

$$I_{REF} = \frac{k_n'}{2}\left(\frac{W}{L}\right)_1 (V_{GS}-V_T)^2(1+\lambda V_{DS})$$

But $V_{DS} = V_{GS}$



$I_{O2} \neq I_{REF}$ unless $(W/L)_1 = (W/L)_2$ and $V_{O2} = V_{DS1} = V_{GS}$