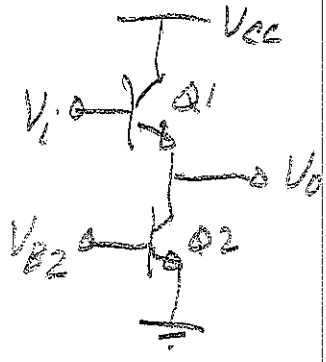
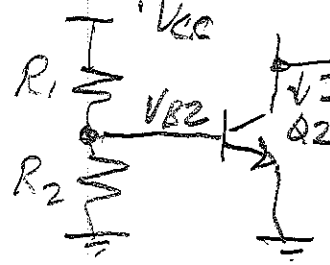
- Current sources for DC biasing and active loads:

Consider a BJT Emitter Follower:



How to generate bias voltage V_{B2}?

One possibility: Resistive Divider



- Ignore I_{B2} for now.

$$V_{B2} = \frac{R_2}{R_1+R_2} V_{CC}$$

But, with resistor variations, V_{B2} may vary from ideal desired value. I_2 is very sensitive to V_{B2}

How much for 10× variation?

$$10 I_2 = I_S e^{V_{BE2}/V_T}; \quad I_2 = 10\, e^{V_{BE1}/V_T}$$

$$\therefore (V_{BE2} - V_{BE1}) = \Delta V_{BE} = V_T \ln(10) = \boxed{60\text{ mV}}$$

∴ 10× current error for every 60 mV of V_{B2} error!

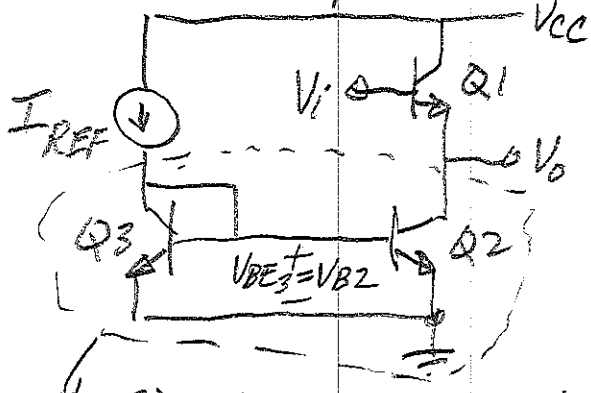
- V_{B2} is a precision voltage ∴ This is a bad design!!!

- Basic principle of precision design ≡ **Replication**

Use same (i.e., ideally identical) device types.

- Exploit very good matching accuracy on ICs

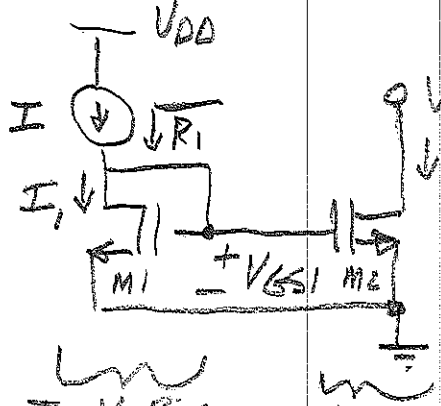
So, use an npn identical to Q2 to generate V_{B2}:



Simple npn current mirror is difficult so one I_{REF} per chip.

Note: Ideally, I_{REF} should be accurate and insensitive to Process, Voltage and temperature (i.e., PVT) variations. This

(A) Consider a simple NMOS current mirror:



- Let's assume M1 and M2 are identical in size and device parameters:
- M1 is diode connected so that $V_{DS1} = V_{GS1}$
- Also, resistance seen by I source is low as desired:

$$R_1 = \frac{1}{g_{m1} + g_{o1}} \simeq \frac{1}{g_{m1}}$$

- Neglect channel-length modulation for now:

$$I = \frac{k_n'}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_T)^2$$

$$\therefore V_{GS1} = \sqrt{\frac{2I}{k_n'\left(\frac{W}{L}\right)_1}} + V_T$$

- M1 always in sat if diode:

$$V_{DS} \overset{?}{\geq} (V_{GS} - V_T)$$

But $V_{DS} = V_{GS}$

$V_{DS} \geq V_{GS} - V_T$ always true

Hence,

$$I_2 = \frac{k_n'}{2}\left(\frac{W}{L}\right)_2 (V_{GS1} - V_T)^2$$

$$= \frac{k_n'}{2}\left(\frac{W}{L}\right)_2 \left[\sqrt{\frac{2I}{k_n'(W/L)_1}} + V_T - V_T\right]^2 = \boxed{\frac{(W/L)_2}{(W/L)_1} I}$$

- Usually design for equal L values (not minimum for analog applications)

Consider some sources of error:

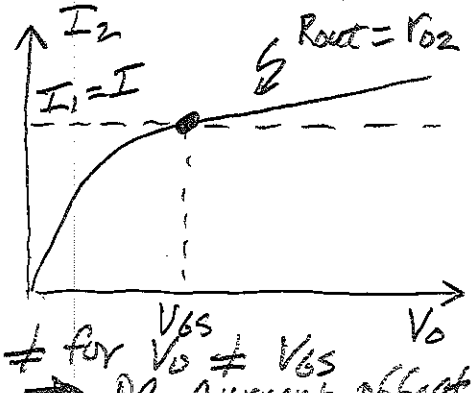
(i) Channel-length modulation (identical devices):

$$I_1 = I = \frac{k'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS1})$$

$$= \frac{k'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{GS})$$

$$I_2 = \frac{k'}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_O)$$

for $V_O \geq (V_{GS} - V_T)$



$I_2 \neq$ for $V_O \neq V_{GS}$

→ DC current offset

(ii) Consider device parameter mismatches:

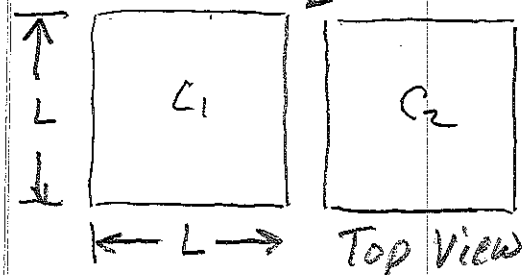
$$I_2 = \frac{K_2'}{2}\left(\frac{W_2}{L_2}\right)(V_{GS}-V_{T2})^2(1+\lambda_2 V_0)$$

$$I = I_1 = \frac{K_1'}{2}\left(\frac{W_1}{L_1}\right)(V_{GS}-V_{T1})^2(1+\lambda_1 V_{GS})$$

$$\therefore \frac{I_2}{I_1} = \frac{K_2'}{K_1'}\left(\frac{W_2}{W_1}\right)\left(\frac{L_1}{L_2}\right)\frac{(V_{GS}-V_{T2})^2}{(V_{GS}-V_{T1})^2}\,\frac{(1+\lambda_2 V_0)}{(1+\lambda_1 V_{GS})}$$

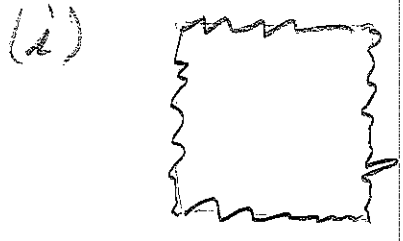
- See 3.5.6.6 – 3.5.6.7 in GM for perturbation analysis
- Make M1 & M2 identical; $W_1 = W_2$, $L_1 = L_2$, etc.

- an aside on device matching in ICs:
- Suppose we want to match two (square) capacitors:

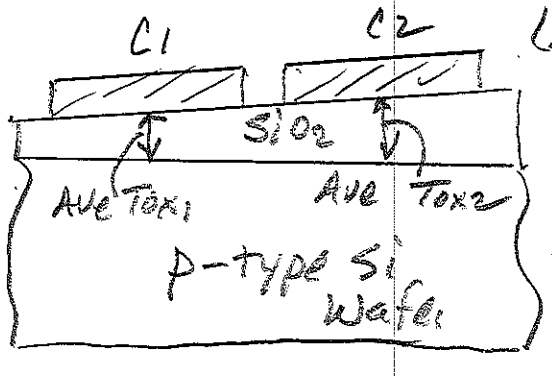


- minimum spacing set by layout rules
- Two major effects on matching accuracy:

(i) edge effects — Due to finite wavelength effects, etching variations, etc. Some average edge uncertainty, σ_L, which is constant and $\neq f(L)$

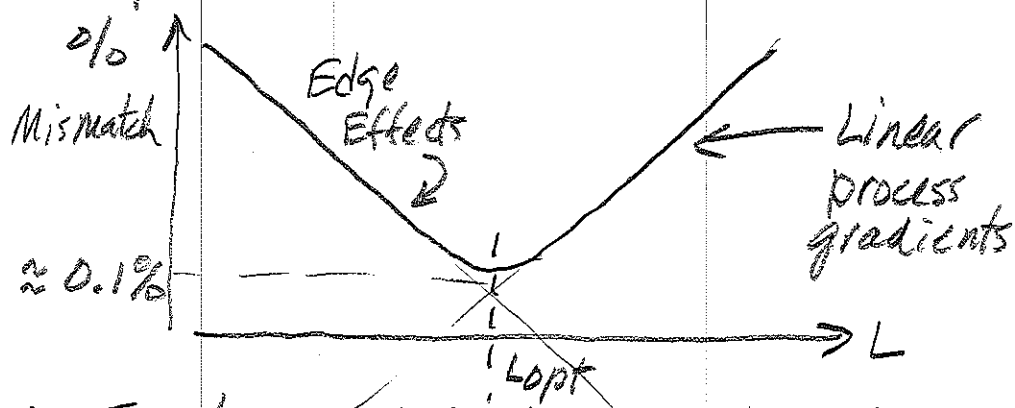


(ii) Global variations (linear) across wafer; e.g. oxide thickness variation



as L increases, the difference between T_{ox1} (ave) and T_{ox2} (ave) increas.

So, considering edge effects and CMOS process gradients, the mismatch between ideally matched pairs looks like this:

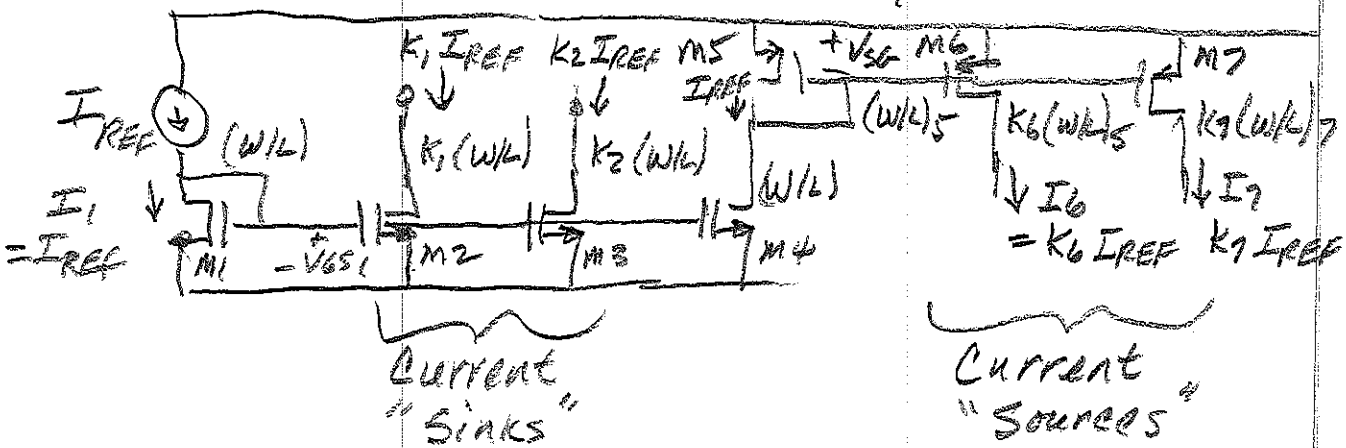


Lopt is Foundry and technology dependent but usually Lopt is about 20 μm.

Suggested Reading:

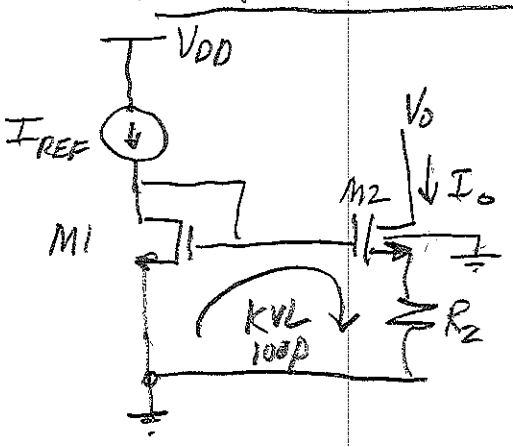
- M. Pelgrom, et al., "Matching Properties of MOS Transistors," IEEE J. Solid-State Circuits, May 1989. (Classic Paper)

- Scaled current copies are easy in CMOS:



(B) Consider NMOS Widlar current sources
(i) For generating small DC bias currents
(ii) For supply-independent DC bias
(iii) For process-tracking opamp frequency compensation of opamps (Later)

(i) Most Common Widlar Configuration:



• One advantage of this topology is increased R_{out} (i.e., it is a "better" current source than the simple one:

$$R_{out} \simeq \underbrace{g_{m2} R_2 r_{o2}}_{\text{improvement factor}}$$

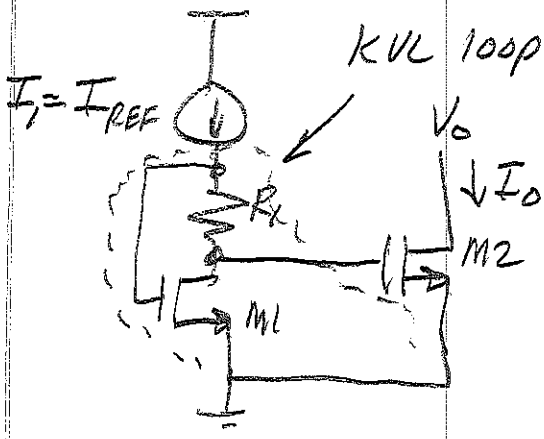
KVL ⟹

$$\sqrt{I_o} = \frac{\sqrt{\frac{2}{k'(W/L)_2} + 4R_2 V_{ov1}} - \sqrt{\frac{2}{k'(W/L)_1}}}{2R_2} \qquad \left(\frac{4.197}{6M}\right)$$

Where $V_{ov1} \equiv (V_{GS} - V_{T1}) = V_{dsat1}$

• One disadvantage is back-gate effect on M2 which is ignored in equation above

(ii) Alternative Widlar Configuration:

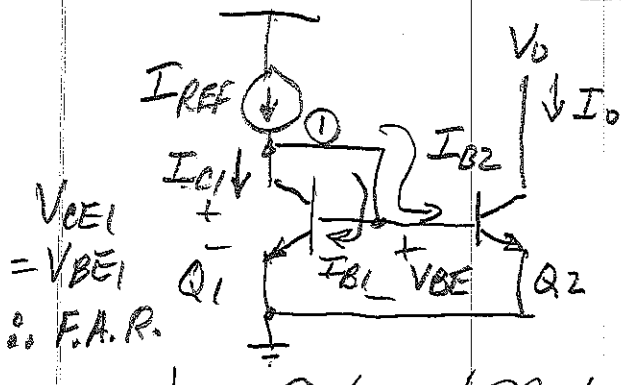


• Advantage: no backgate effect on M2
• Disadvantage: $R_{out} = r_{o2}$

KVL: $V_{GS1} - I_1 R_1 - V_{GS2} = 0$

$$\therefore \sqrt{I_o} = \sqrt{\frac{k'(W/L)_2}{2}} \left[\sqrt{\frac{2I_1}{k'(W/L)_1}} - I_1 R_1 \right]$$

(C)(i) npn Simple current mirror:



- Q_2 in F.A.R. for $V_O \geq V_{SAT_2} \simeq 0.2\,V$
- $I_{C1} \simeq I_{S1}\, e^{V_{BE}/V_T}$
- $\therefore V_{BE} = V_T \ln\left(\frac{I_{C1}}{I_{S1}}\right)$
- But, $I_{C1} \neq I_{REF}$ due to base current errors

KCL at ①: $I_{REF} = I_{C1} + I_{B1} + I_{B2}$

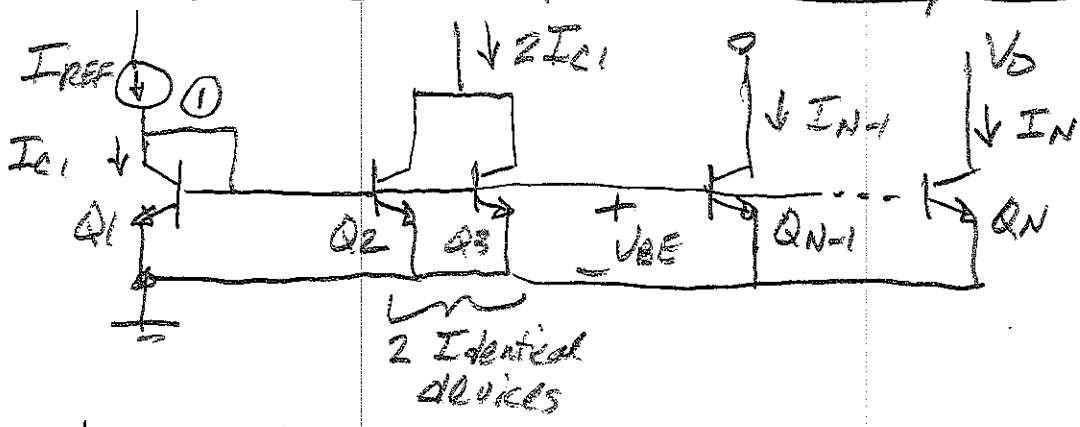
Assume Q_1 and Q_2 are identical ➡ $I_O = I_{C1}$

$$\therefore I_{REF} = I_{C1} + \frac{I_{C1}}{\beta_D} + \frac{I_{C1}}{\beta_O} = I_{C1}\left(1 + \frac{2}{\beta}\right)$$

$$\therefore \boxed{I_{C1} = \frac{I_{REF}}{1 + \frac{2}{\beta}}}$$

← Few % error in Simple npn mirror

(ii) Consider multiple scaled outputs:



KCL at ①: $I_{REF} = I_{C1} + I_{B1} + I_{B2} + I_{B3} + \cdots I_{BN}$

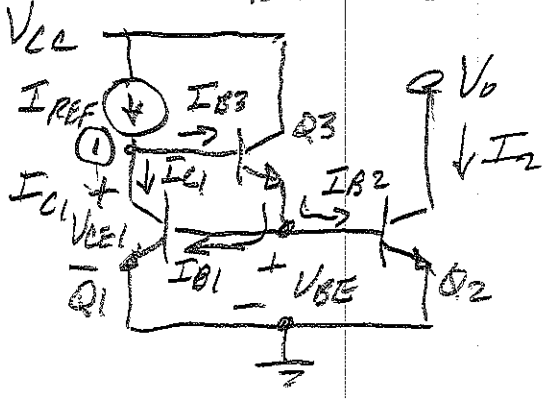
$$= I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_{C1}}{\beta} + \cdots \frac{I_{C1}}{\beta}$$

$$= I_{C1}\left(1 + \frac{N}{\beta}\right)$$

$$\therefore I_{C1} = \left(\frac{I_{REF}}{1 + N/\beta}\right)$$ ← can be large if N is large.

(D) npn current mirror with Beta helper:

Idea: Take advantage of current gain of BJT to make $I_{C1} \simeq I_{REF}$



- Again, Q2 in F.A.R. for $V_O > V_{SAT}$
- Now, $V_{CE1} = V_{BE1} + V_{BE3}$ so Q1 also F.A.R.
- Assume $I_2 = I_{C1}$ $\left(\begin{smallmatrix} Q_1 = \\ Q_2 \end{smallmatrix}\right)$

KCL at ①:

$$I_{REF} = I_{C1} + I_{B3}$$

$$= I_{C1} + \frac{I_{E3}}{\beta_3 + 1}$$

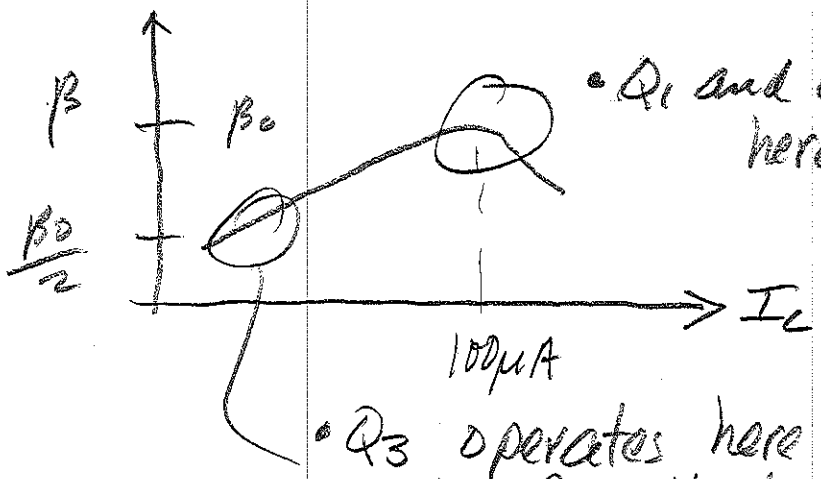
$$= I_{C1} + \frac{(I_{B1} + I_{B2})}{(\beta_3 + 1)}$$

$$= I_{C1} + \frac{2 I_{C1}}{\beta_1 (\beta_3 + 1)}$$

$$\therefore I_{C1} = \frac{I_{REF}}{1 + \frac{2}{\beta_1 (\beta_3 + 1)}} \simeq \boxed{\frac{I_{REF}}{1 + \frac{2}{\beta^2}}}$$

Very small error

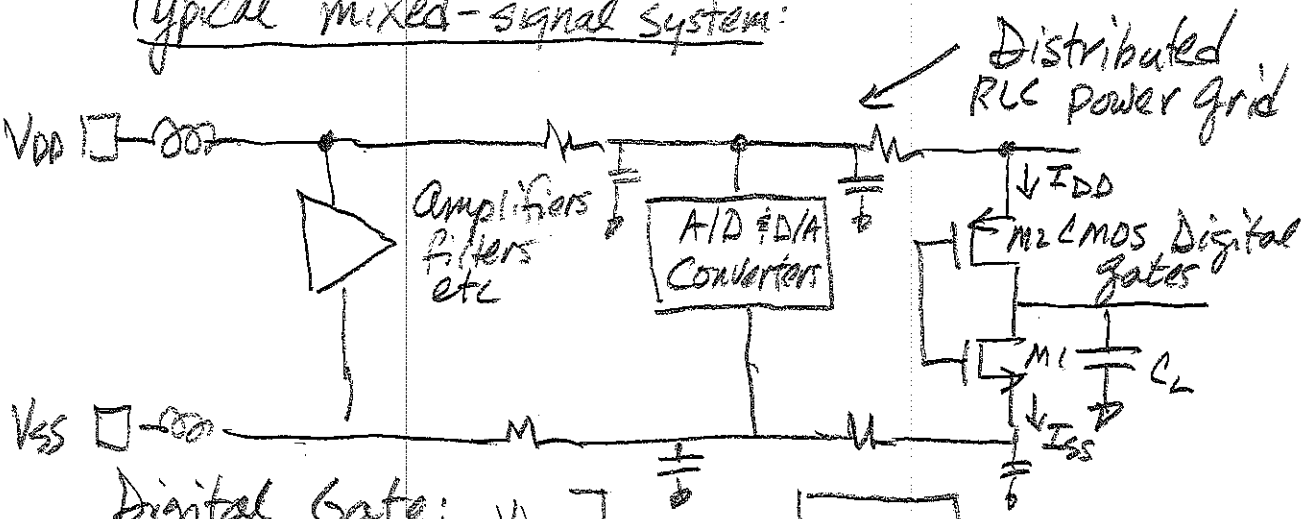
But, be careful because β is not constant vs I (Fig. 1.15 GM):



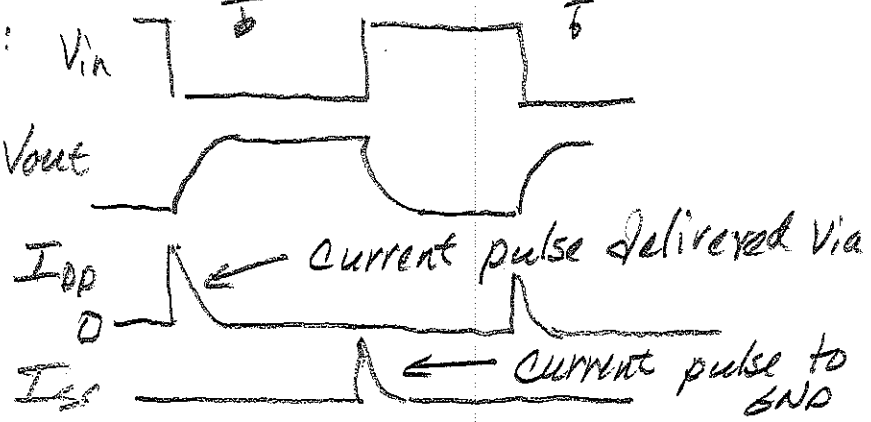
- Q_1 and Q_2 may operate here
- Q_3 operates here where β is significantly lower

- **Supply and Temperature-independent Biasing:**
  - As battery voltage or supply voltage changes,
    - Amplifier gain changes
    - Power consumption changes
    - Amplifier bandwidth changes
    - Oscillator frequency changes
  - Similar issues as temperature changes
  - Short-term supply voltage variations
    - Power supply digital switching noise can couple into precision analog circuits.

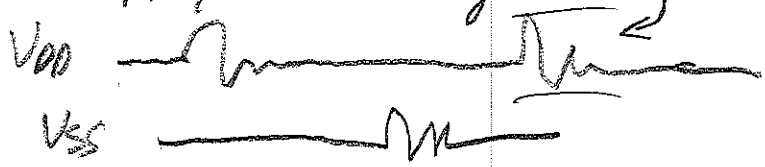
Typical mixed-signal system:



Digital Gate:



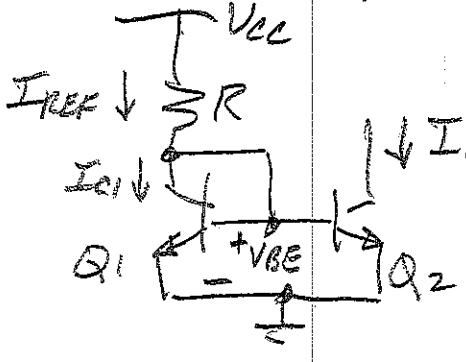
Result: Power supply noise may be 100 mV or more



- General Sensitivity function:

$$S_x^y = \frac{x}{y}\frac{\partial y}{\partial x} \equiv \text{Sensitivity of variable } y \text{ w.r.t. variable } x:$$

- Consider simple current source:



- Neglect base currents
- Q_1 identical to Q_2

$$\therefore I_{REF} = I_{C1} = I_O = \frac{V_{CC} - V_{BE}}{R}$$

Further, assume $V_{CC} \gg V_{BE}$ ($\simeq 5V$) ($\simeq 0.7V$)

$$I_O \simeq \frac{V_{CC}}{R}$$

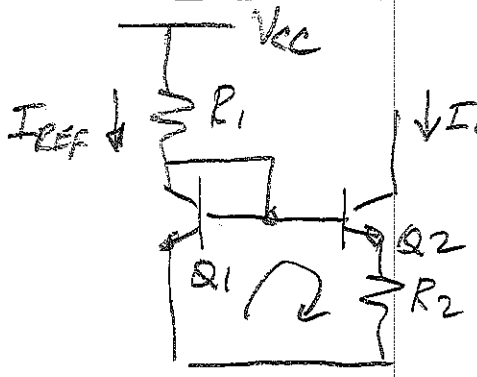
$$\therefore S_R^{I_O} = \frac{R}{I_O}\frac{\partial I_O}{\partial R} = \frac{R}{I_O}\left(-\frac{V_{CC}}{R^2}\right) = \underline{\underline{-1}}$$

This means a 20% increase in R, for example, gives a −20% change in I_O ➡ Bad sensitivity!!

Also, $$S_{V_{CC}}^{I_O} = \frac{V_{CC}}{I_O}\frac{\partial I_O}{\partial V_{CC}} = \frac{V_{CC}}{I_O}\left(\frac{1}{R}\right) = \underline{\underline{+1}}$$

∴ Very bad supply sensitivity.

- Consider Sensitivity of Widlar Current source:



KVL: $V_{BE_1} - V_{BE2} = I_O R_2$

$$\therefore V_T \ln\frac{I_{C1}}{I_S} - V_T \ln\frac{I_O}{I_S} = I_O R_2$$

$$V_T \ln\frac{I_{C1}}{I_O} = I_S R_2$$

But $I_{C1} = I_{REF}$ (neglect base currents)

$$\text{So, } V_T \ln\frac{I_{REF}}{I_O} = I_O R_S$$

$$V_T \left[\ln I_{REF} - \ln I_O \right] = I_O R_2$$

Now, take derivative with respect to V_{CC}:

$$V_T \left[\frac{1}{I_{REF}} \frac{\partial I_{REF}}{\partial V_{CC}} - \frac{1}{I_O} \frac{\partial I_O}{\partial V_{CC}} \right] = R_2 \frac{\partial I_O}{\partial V_{CC}}$$

$$\Rightarrow \boxed{\frac{\partial I_O}{\partial V_{CC}} = \frac{\frac{V_T}{I_{REF}} \frac{\partial I_{REF}}{\partial V_{CC}}}{R_2 + \frac{V_T}{I_O}}}$$

$$\therefore S_{V_{CC}}^{I_O} = \frac{V_{CC}}{I_O} \frac{\partial I_O}{\partial V_{CC}}$$

$$= \frac{V_T \left[\frac{V_{CC}}{I_{REF}} \frac{\partial I_{REF}}{\partial V_{CC}} \right]}{V_T + I_O R_2}$$

Note: $S_{V_{CC}}^{I_{REF}} = +1$ (From previous page assuming $I_O = I_{REF}$)

Finally, $$S_{V_{CC}}^{I_O} = \boxed{\frac{1}{1 + \frac{I_O R_2}{V_T}}}$$

Example: $I_O R_2 = V_{BE1} - V_{BE2} = \Delta V_{BE} = 200mV$

$$\therefore S_{V_{CC}}^{I_O} = \frac{1}{1 + \frac{200mV}{25mV}} = \frac{1}{9}$$

- Much better than simple current mirror !!

How can we do better? Use another voltage rather than V_{CC} to generate I_O:

- V_{BE} - Base-Emitter Voltage
- Zener Diode Voltage
- V_T - MOS threshold
- $V_T - kT/9$
- Silicon Bandgap Voltage