EE 140/240A
Fall 2014
D.J. Allstot

Lecture 1 -Admin and Overview

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- Announcements
  - Class account sheet
  - Course Details
  - Course Syllabus

- Lecture Topics:
  - Op-amp examples
  - Review -notation and building blocks
  - Ideal op-amp

- About me:
  - Ph.D. UC Berkeley 1979
  - Prof. at U. Washington 1999-2012
  - Visiting Prof. at Stanford 2012
  - Mackay Prof. in EECS at UCB 2013 -
  - Research: Radio Frequency, mixed-signal, analog integrated circuits; ultra-low power biomedical circuits; compressed sensing systems)

COURSE INFORMATION

Instructor:

Prof. David J. Allstot, 564 Cory Hall, Tel: (510) 559-0195
e-mail address: allstot@berkeley.edu
Office Hours: TuTh 4-5 p.m. and 6:30-7:30 p.m. in 564 Cory

Teaching Assistants (TA's):
TA: Pi-Feng Chiu
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Office Hours: TBD, 125 Cory Hall

Lecture: TuTh 5:00-6:30 p.m. in 247 Cory

Discussion Sections:

Section 101: Mon, 3-4 p.m. in 247 Cory
Section 102: Mon, 4-5 p.m. in 247 Cory

Laboratory Sections:

Section 11: Monday, 9 am-12 pm in 125 Cory
Section 12: Wednesday, 12 - 3 pm in 125 Cory

Office Hours:

Office hours are the primary mechanism for individual contact with Professor Allstot and the TAs. All students are strongly encouraged to make use of office hours.

Class Discussions and Announcements:

We will use Piazza extensively this term for discussions and announcements.

Class discussion: https://piazza.com/berkeley/Fall2014/ee140/home

Integrated Circuits have seen tremendous growth over the past forty years and promise to continue that growth for many years to come. The year 2010 had already seen silicon CPU chips using more than 2 billion transistors, and Moore's Law promises even larger transistor counts in the coming years. Analog integrated circuits are becoming ever more sophisticated and important, since they provide the very important function of interfacing many data acquisition and signal processing systems with purely digital computers. In addition, as mixed-mode analog/digital systems become more important in many consumer products, such as cellular communications and wireless data acquisition systems, the design and analysis of analog integrated circuits has become a very important requirement for many designers of VLSI systems. One major component in many of today's analog electronic systems is the operational amplifier. The op-amp is used as a circuit block in systems such as analog-to-digital and digital-to-analog converters, switched-capacitor functions, signal processing systems, integrated circuit filters, and virtually all systems where amplification of input signals is needed. Indeed, the op-amp is probably the most commonly used analog circuit block.

As a result, it is important for students interested in electronic circuit design and analysis to have a thorough knowledge of the design and analysis of the operational amplifier. This course will examine the technology and circuit techniques associated with integrated monolithic amplifier circuits and the challenges that lie ahead in their development. The goal is to achieve a basic understanding and knowledge of the driving and limiting factors in circuit performance, of circuit design techniques, and of fabrication techniques and technology issues important to integrated amplifier circuits in general, and to op-amps in particular.

The first part of the course reviews the small-signal models of both Bipolar Junction Transistor (BJT) and Metal-Oxide-Semiconductor (MOS) transistors. The course assumes that students have had a significant amount of experience in the analysis and design of discrete BJT amplifiers, and some experience in the design and analysis of MOS amplifiers. Consequently, MOS amplifier stages will be emphasized initially and more lab experiments will be geared towards illustrating specifically the design of MOS amplifiers. BJT and MOS multi-transistor amplifiers are reviewed next with an emphasis on inspection analysis of multi-transistor circuits. After covering basic material on transistor amplifiers, we will review the application of transistors in the design of various basic analog circuit blocks that are utilized in the implementation of a complete integrated operational amplifier circuit. These circuit blocks include current sources and current mirrors, level shifters, active loads, and differential amplifier stages. These circuit blocks are needed in the design and analysis of many amplifier circuits, and are particularly required for the design and analysis of op-amps. Although much of the lecture coverage will be on MOS op amp design, you will assemble and design an operational amplifier in the laboratory using several different circuit blocks based on BJT devices, which are more robust for use in a laboratory setting. Since it is impractical to build an actual CMOS op-amp in the laboratory using off the shelf components, you will be given a design project that involves the design and simulation of a CMOS op-amp using available CAD tools. This laboratory will be a software lab assignment, and will focus on the design tradeoffs involved in the design of CMOS op-amps. There will be no hardware labs during this time. Note that the design project will be due before the end of the semester, unless circumstances dictate otherwise. An important topic in the design of any amplifier circuit is that of feedback and amplifier stability, and this course will spend sufficient time discussing feedback and the use of feedback techniques to stabilize the response and performance of amplifier circuits. The course concludes with coverage of some practical issues in analog circuit, such as stability against variations in power supply and temperature, for which supply and temperature independent bias references will be needed.

Lectures are intended to discuss and supplement the material in the text and the laboratory experiments. A number of suggested reference books are listed below that should supplement the material not covered in the textbook. Problem sets will attempt to emphasize important points. Students will analyze and simulate circuits using SPICE, and analyze problems related to fabrication of analog ICs. Both hardware and software labs will be assigned to familiarize students with the design aspects of amplifier circuits in general, and op-amps in particular.

Lectures and discussion, 4 units.

Prerequisites:

The prerequisites for this course are EE 105 and some aspects of EE 20N. It is assumed that you are familiar with the following topics:

- **Basic network theory**
- **Basic linear systems theory (Fourier and Laplace transforms, Bode plots)**
- **The use of small-signal models in the analysis and design of BJT and MOS amplifier circuits**
- **Analysis of single-and multi-transistor amplifiers with BJTs and MOS (including common-emitter (source), common-collector (drain), common-base (gate), cascode, cascade, Darlington, etc.)**
- **Elementary semiconductor physics and device operation for pn junctions, bipolar junction transistors (BJTs), and MOS field-effect transistors (MOSFETs)**

Familiarity with integrated circuit fabrication techniques is helpful, but not necessary. We will review IC fabrication techniques whenever needed.

Texts:
Required: Gray, Hurst, Lewis, Meyer, *Analysis and Design of Analog Integrated Circuits*, 5thEdition, John Wiley & Sons, 2009.

Various material to be distributed throughout the course.

Recommended: B. Razavi, *Design of Analog CMOS Integrated Circuits*, First Edition, McGraw Hill, 2001.
Note that this text was used for previous renditions of this course, so is still very relevant as supplemental reading, especially for MOS circuit design.

Reading Assignments:

Reading assignments include sections of the required textbook, distributed readings, and supplementary notes handed out in lecture. Reading assignments are indicated in the COURSE SYLLABUS and will also be included in problem assignments where appropriate. Supplementary notes will be handed out for topics where lecture coverage is substantially different from the textbook. Students are responsible for all material in the reading. In particular, the scope of coverage for problem sets, the midterm, the project, and the final examination includes the reading assignments as well as lecture material.

Problem Sets:

There will be a number of problem sets over the course of the semester, assigned approximately once per week. Each new problem set will normally be posted on the course website the day the previous problem set is due. The problem sets will be due on Friday’s at 1 pm, and should be turned in to the EE140/240A box near 140 Cory (TI lab). Solutions will be posted on the web.

Laboratory:

The laboratory exercises are intended to reinforce the material covered in lecture and in problem sets. Laboratory sessions will meet as needed, except for those weeks indicated on the course syllabus. For all the hardware labs the students will typically work in pairs; for the CMOS op-amp design problem, students will work individually. The topics covered in the labs are coordinated with the lectures, but will lag somewhat.

Handouts will be distributed for each lab experiment. The handouts will explain the experiments that need to be carried out in the laboratory. Each student is responsible for reading the handout prior to coming to the laboratory and preparing any material that is needed for the successful and timely completion of the lab experiments. Remember that the lab facilities are shared with other courses, many of which require more consistent use of the laboratory. Therefore, make sure that you prepare yourself so that you can finish the experiments in the allotted time. You are responsible for any preparation, and we will not ask you for any specific pre lab reports.

Lab reports are required after the experiments are actually conducted in the laboratory. The due dates for the lab reports will be announced when the handout is passed out. For the labs conducted in groups of two, each student should turn in a separate report. The format of the report will vary from lab to lab. However, generally you are required to write a report that discusses the objectives of the lab experiments, shows any hand calculations and design procedures, presents computer simulations, summarizes any measurements that were performed to carry out the experiment, and provides a discussion section which is where you will discuss the particular lab experiment. You should use these lab experiments and the reports as a means to understand the topic, to think about the issues involved in amplifier circuit design, and to elaborate and discuss your findings beyond what was specifically asked in the lab handouts. In other words, you will not always be asked to answer specific questions listed in your handout. Rather, you should think about the lab and your results and provide a free format discussion of what you think was significant. Most of you have substantial circuit analysis and design experience by now, and you should be able to provide a more detailed discussion of your own. We will try to give you as much information about the grading of the lab reports so that you know how to prepare your reports.

One of the main purposes of the course is to teach some of the tradeoffs involved in amplifier circuit design and analysis. I would have liked to make all of the lab experiments "design" experiments. However, it is not possible to do that because we are also introducing several important topics in this course, such as feedback and stabilization. As a result, we will need to conduct some standard pre-arranged lab experiments so that you can see these effects in a real circuit. We have tried to include design wherever possible so that you can gain some design experience. The CMOS op-amp design lab will have a major design content. It should be noted that these design problems require a considerable amount of time to complete, and take the place of two or more regular assignments. They also receive a grading weight roughly in proportion to the time allotted for completion. Students are *strongly* encouraged to start on these assignments as soon as they are made available. At least 10% of any lab report grade will be based on the quality of the report. The “document quality” category is intended to encourage students to prepare their reports in a manner that makes them readable and easy to evaluate properly. Laboratory reports need not be typed, nor will typing result in additional credit in the “document quality” category, but carelessly prepared material will result in a loss of credit.

The series of lab experiments to be carried out in this course at this point in time are listed below, with the grade that each lab will carry. Be warned that these are tentative, and changes may be made during the course of the semester (e.g., a lab may be eliminated if time constraints dictate).

Assignment	*Points*
Lab 1: MOS Amplifier Analysis & Design	200
Lab 2: Discrete BJT Op-Amp Analysis and Design	300
Lab 3: CMOS Op-Amp Design Project	900
TOTAL	***1400***

Note that some labs are multi-week labs, like lab #3, and therefore carry a heavier work load and constitute a larger percentage of the overall lab grade. Laboratory performance is very important and poor attendance, disruptive behavior, chronic lateness, etc. will result in a loss of credit when lab reports are graded.

As mentioned above, the design project lab involves the design of a CMOS op-amp and gives you an opportunity to exercise engineering judgment and learn about the *design* process (as compared to *analysis* that will be the emphasis of this course). The design problem will involve the design of a CMOS operational amplifier with a given set of specifications. Students are expected to complete a hand design that is verified by computer simulation using SPICE. CMOS operational amplifiers are one of the most important circuit blocks in many analog systems and the experience you gain throughout this design project will be extremely invaluable to you in the future.

Midterm:

There will be a midterm exam in this course to be held on the date shown in your COURSE SYLLABUS. We will try to adhere to this date so much as possible. The midterm will be a 1.5 hour exam and will be closed book and closed notes. More information on the exam will be provided later.

Final Exam:

The final exam will be comprehensive, covering all of the material in the course. This includes everything covered in problem sets, lectures, and readings. The exam will be held during the Examination Period at the scheduled time. The date is shown in your course syllabus.

Computer Accounts/CAD Tools:

You will receive a class account and password on a document handed out in class. This account will give you access to all of the necessary software for your course work.

Grading Policy:

Problem Sets: 15%
Laboratory/Projects: 30%
Midterm Exam: 25%
Final Exam: 30%

Date	Material to be Covered	HWs	Labs
Aug. 28	Administrative Information, Introduction/Overview; Op amps		Week 1: No Lab
2	Device Operation & Models; BJT & MOS: GM 1.1-1.6; R Chap. 2		Week 2: No Lab
4	Device Operation & Models; Inspection Analysis: GM 1.1-1.6; R Chap. 2		"
9	BJT Inspection Analysis: GM 3.1-3.3; R 3.1-3.4, 6.1-6.4		Week 3: No Lab
11	MOS Inspection Analysis: GM 3.4; R 3.5-3.6	HW 1 Due	"
16	Frequency Response Inspection Analysis I: GM 7.1-7.3; R 6.5		Week 4: Lab 1 1-Tx MOS Amp
18	Frequency Response Inspection Analysis II: Active Loads: GM 4.3	HW 2 Due	"
23	Active Loads: 1-TX and Multi-TX Loads: GM 4.3		Week 5: Lab 1 (cont.)
25	Current Sources: GM 4.2: R 5.1-5.2	HW 3 Due	"
30	Supply & Temperature Indep Biasing: GM 4.4.2-4.4.3; R Chap 11		Week 6: Lab 2-1 Diff Pair Design & Analysis
Oct. 2	High-Swing Current Sources I: GM 4.2.5.2; R 5.1-5.2	HW 4Due	"
7	High-Swing Current Sources II: GM 4.2.5.2; R 5.1-5.2		Week 7: Lab 2-2 2nd Gain Stage Design
9	Current Source Matching: GM A.4.1	HW 5 Due	"
14	Op Amps: Op Amp Feedback Circuits: GM 6.1-6.2, 3.5; R 4.1-4.4		Week 8: Lab 2-3 Complete opamp Analysis
16	Op Amps: SCP; Current Mirror Load; GM 4.3.5	HW 6 Due	"
21	Op Amps: Input Offset Voltage; Finite Gain-BW Product, Frequency Response in Feedback: GM 3.5.6, A.4.2, 9.2		Week 9: Lab 3 CMOS opamp design project
23	Op Amps: High Gain Designs; GM 6.3-6.7; R 9.3-9.4	HW 7 Due	"
28	Op Amps: Swing, Compensation and Slew Rate (a 1st pass); GM 9.4.1-9.4.2, 9.6.1-9.6.2; R 9.7-9.8		Week 10: Lab 3 Work on Project
30	**MIDTERM EXAMINATION**		**"**
Nov. 4	Op Amps: Output Stages; GM 5.1-5.5		Week 11: Lab 3 Work on Project
6	Compensation: Stability of Feedback Circuits, Narrowbanding; GM 9.4; R 10.1-10.3		"
11	**ACADEMIC HOLIDAY – NO CLASS**		**Week 12: Lab 3 Work on Project**
13	Compensation: Pole-Splitting and Pole-Zero Plots; GM 9.4-9.5; R 10.4	HW 8 Due	"

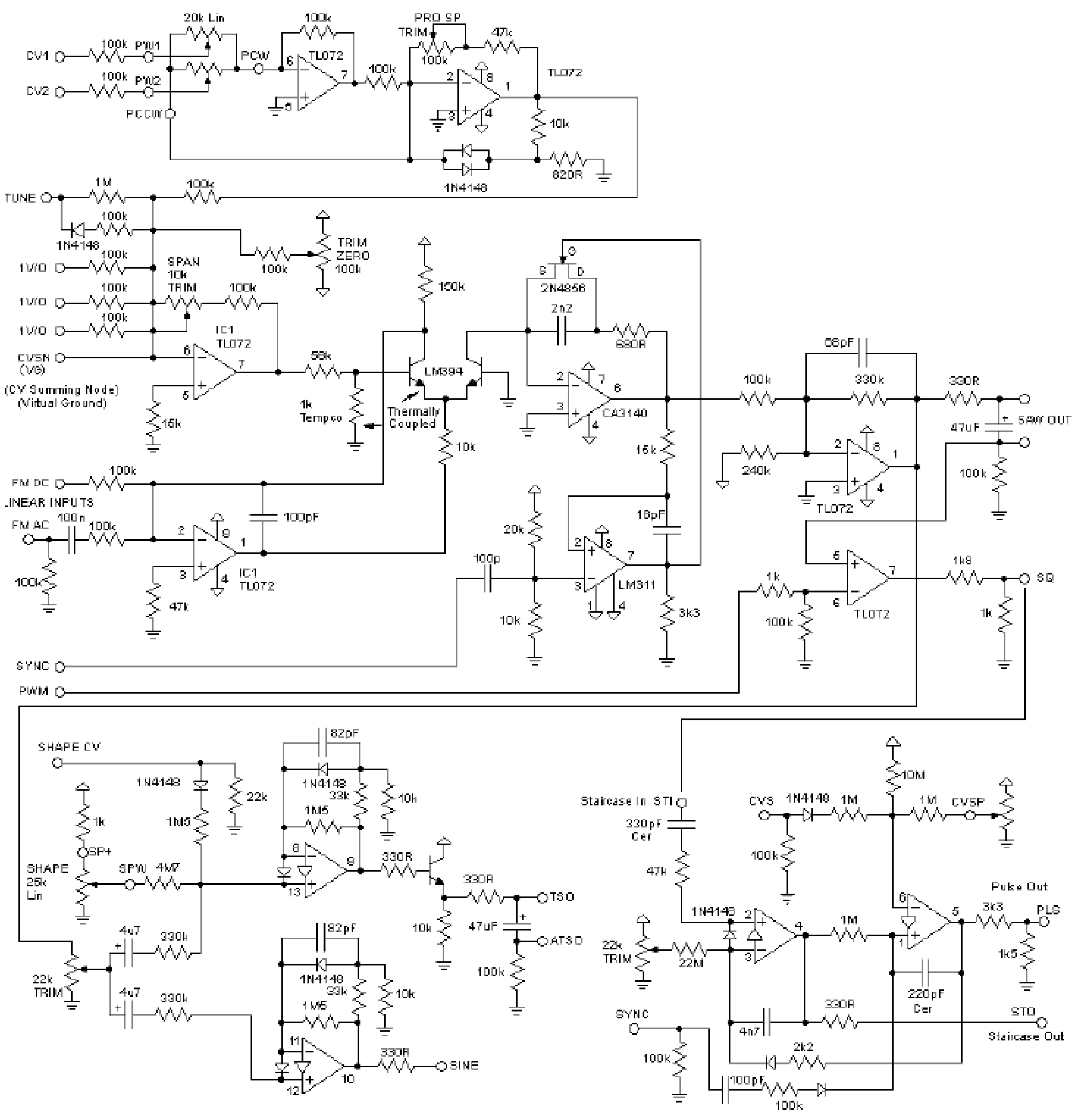
18	Compensation: For CMOS Op Amps, Choosing C_C; GM 9.4.3-9.4.5: R 10.5-10.6		Week 13: Lab 3 Work on Project
20	Compensation: CMOS Op Amp RHP Zero; GM 9.4.3; R 10.5-10.6	HW 9 Due	"
25	Slew Rate: GM 9.6 Settling Time and PSRR; Handout; R 9.9		Week 14: Lab 3 Work on Project
27	**THANKSGIVING HOLIDAY – NO CLASS**		**"**
Dec. 2	Feedback I: Pros and Cons; Inspection Analysis of Feedback Circuits, Influence of I/O Impedance; Handout; GM 8.1-8.2, 8.4; R 8.1-8.2		Week 15: Lab 3 Work on Project
4	Feedback II: Feedback Loading; GM 8.5-8.6; R 8.1-8.3	HW 10 Due	"
9	**READING/REVIEW/RECITATION**		**Week 16**
11	**"**	**Project Due**	**"**
18	**FINAL EXAMINATION 11:30 – 2:30 P.M. (Exam Group 18)**		

Homeworks are due at 1 pm on Fridays.

This term we will be using Piazza for class discussion. The system is highly catered to getting you help fast and efficiently from classmates, the TAs, and myself. Rather than emailing questions to the teaching staff, I encourage you to post your questions on Piazza. Find our class page at: https://piazza.com/berkeley/Fall2014/ee140/home

Lecture 1 -Op-Amp Examples

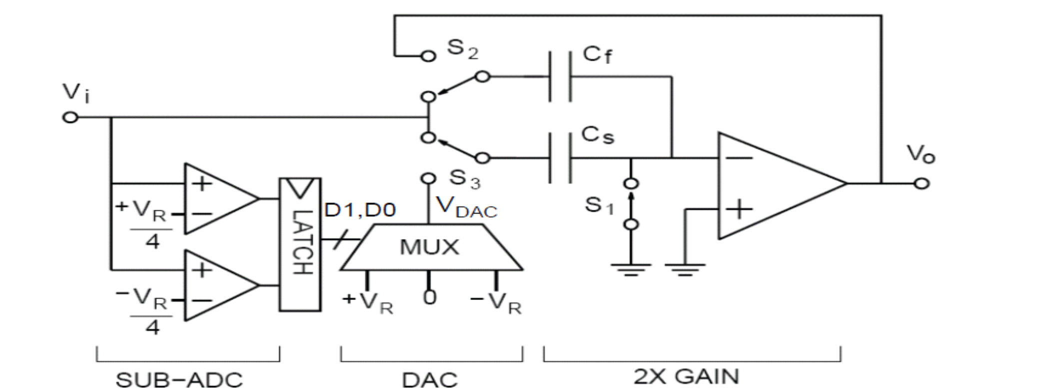
Used in instrumentation, measurement tools, guitar-amplifiers, A/D converters, RF-chains (buffers, AGC), supply regulation



Pipeline A/D Converter Stage

- Switched-cap circuits

1.5-Bit Stage Implementation Example



Ref: A. Abo, "Design for Reliability of Low- voltage, Switched-capacitor Circuits," UCB PhD Thesis, 1999

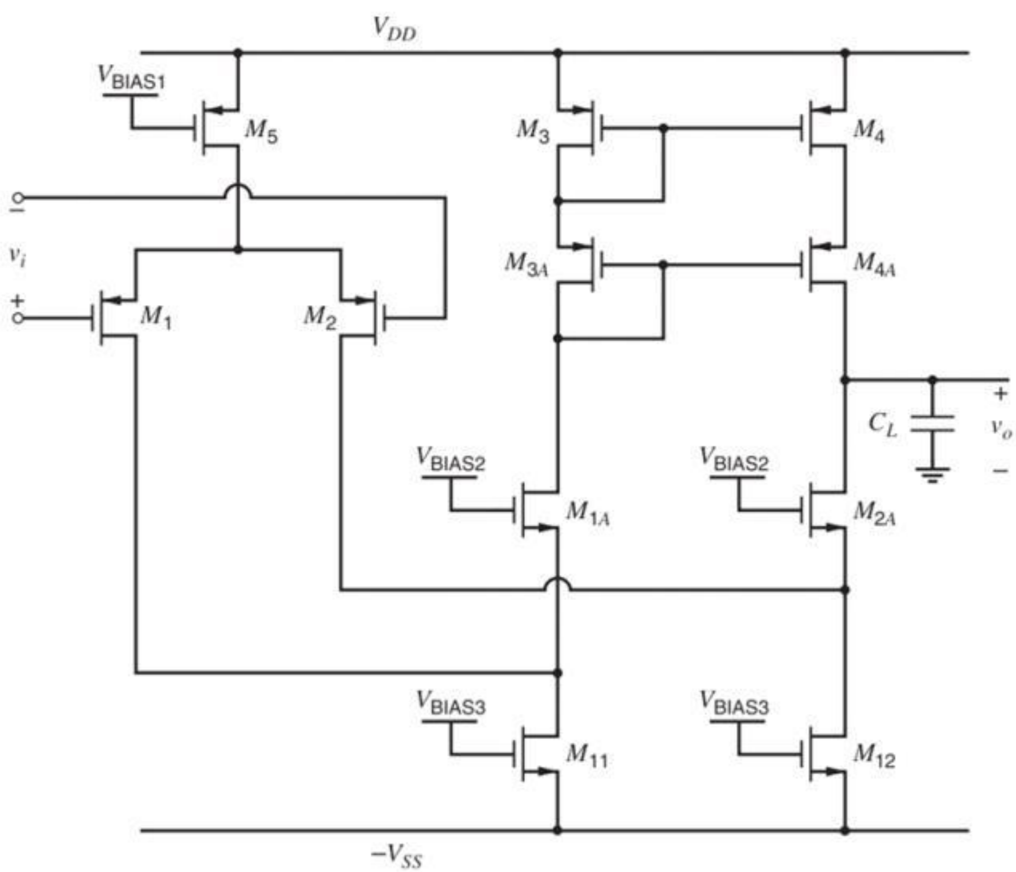


Fig. 6.28

G&M

Folded-Cascode CMOS Op-Amp

741 Op-Amp, industry workhorse