

**INFORMATION ABOUT THE FINAL EXAM****Office Hours:**During RRR week:

We will hold regular office hours throughout RRR week.

During Finals week:

During Finals Week, we will be holding the following office hours:

*Monday, Dec. 14:*

Hao-Yen Tang	11-12 noon
Prof. Nguyen	2-3 p.m.
Alper Ozgurluk	4-5 p.m.

*Tuesday, Dec. 15:*

Prof. Nguyen	11-12 noon
Alper Ozgurluk	2-3 p.m.
Hao-Yen Tang	4-5 p.m.

**Review Session:** (given by your TA's)

Monday, Dec. 14, 9-11 a.m., 521 Cory

**Date of Exam:**

Wednesday, Dec. 16, 8-11 a.m. (sharp)

**Place:**

150 GSPP (Goldman School of Public Policy)

**General Information:**

The exam will be closed book, but you will be allowed two 8.5"×11" sheets on which you can write anything you would like, front and back. Bring a calculator to the exam. You will be provided with exam sheets with enough space to put all your work on these sheets. You should show and include all your work on the exam sheets. (This insures that no pages are missed when we grade.) The exam will consist of a few problems, each with a number of parts.

During the exam, make appropriate engineering decisions and approximations in order to simplify your analyses so that you can do the problems quickly and with fewer errors. In other words, the use of inspection analysis (where applicable) is encouraged. If you are asked to write equations, write the full equation, e.g., neglect nothing, unless they were specified as zero or infinity.

**Material to be Covered:**

Reading in Gray & Meyer, class lecture notes, handouts, and homeworks. The exam is meant to include all material covered so far in the class. You might pay more attention to the following areas:

1. Multiple transistor amplifier circuits, for both BJT and MOS transistors, including cascodes and cascades, either actively or passively loaded. Be able to determine bias points, gain, impedance, and frequency response.
2. Differential pair amplifiers, either actively or passively loaded, including such concepts as biasing, differential-mode gain, common-mode gain, CMRR, half-circuits, and various impedances.
3. Transistor current sources, including ability to determine output current, output resistance, and output swing for a circuit using a given (possibly unfamiliar) current source.
4. Basics of output stage design, including Class A and Class B designs.
5. Derivation of input offset voltages and currents for unfamiliar circuits.
6. Compensation design and techniques, including an understanding of feedback concepts (e.g., closed-loop gain, loop transmission, etc. ...), phase margin, narrowbanding, and pole splitting.
7. Slew rate design, including techniques for maximizing slew rate in amplifiers.
8. Design of operational amplifier circuits, in either bipolar or MOS technology (or both), including biasing and all aspects of small-signal and large-signal performance. Be able to determine common-mode input range, power supply rejection ratio, common-mode rejection ratio, slew rate, phase margin, input offset voltage, as well as gain, frequency, and impedances. In addition, be prepared to design an op amp given a constraining set of specifications.
9. Analysis of general feedback circuits, including an understanding of feedback connection types, feedback loading, the four general amplifier types and their ideal characteristics, and biasing via feedback.

Needless to say, although this exam is centered upon the above concepts, you are also responsible for understanding the required prerequisite background, such as small-signal analysis, Bode plots, device models, etc. Work fast on the exam, making reasonable approximations as necessary to simplify problems. (Remember, the ability to simplify a difficult problem is one of the keys to successful circuit analysis.)