

PROBLEM SET #1

Issued: Tuesday, Aug. 27, 2015

Due (at 8 a.m.): Thursday, Sep. 10, 2015, in the EE 140/240A HW box near 125 Cory.

1. The basic quadratic IV relationships are useful for understanding the DC behavior of MOS transistor circuits. However, any decent circuit model should also take into account the capacitances associated with the devices to accurately predict the AC behavior. Consider the following physical structure of an MOS transistor. Fig. PS1.1 provides the cross section and top views for ease of visualization. Please refer to Table PS1.I for definitions and numerical values for the geometric or process parameters used in the problem.

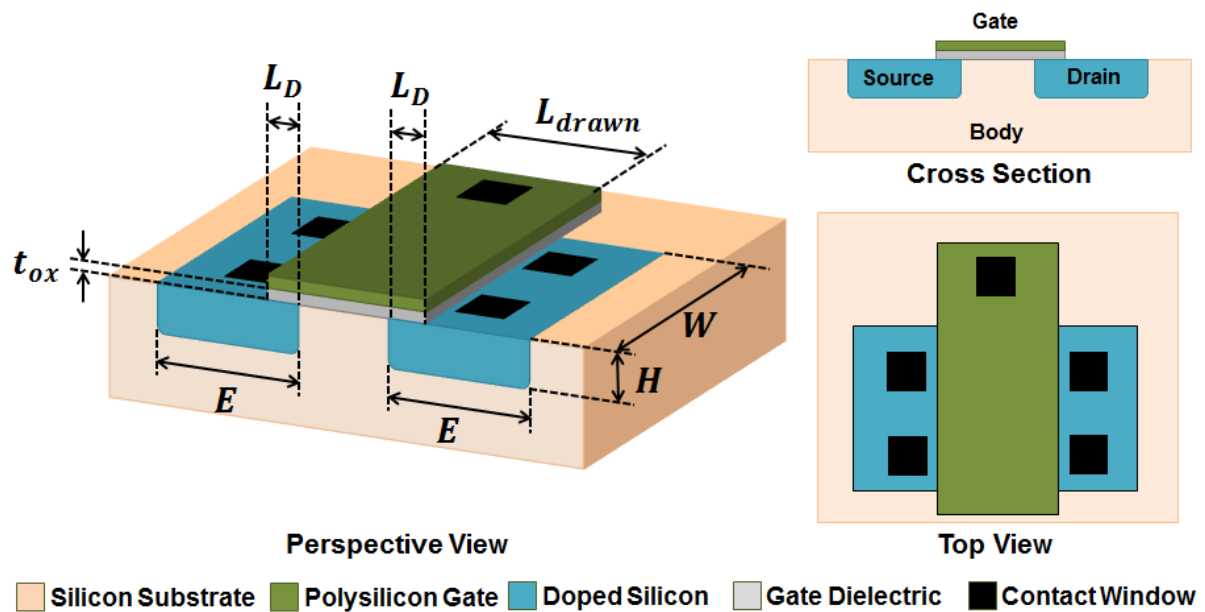


Fig. PS1.1

Parameter	Value	Parameter	Value
Drain/Source Width (W)	$8\mu m$	Gate Dielectric Perm. (ϵ_{ox})	3.9
Drain/Source Length (E)	$1\mu m$	Silicon Permittivity (ϵ_{Si})	11.7
Drain/Source Thickness (H)	$200nm$	Substrate Doping Den. (N_{Sub})	$10^{16}cm^{-3}$
Diffusion Length (L_D)	$100nm$	Electron Mobility (μ_n)	$1400cm^2/Vs$
Drawn Channel Length (L_{drawn})	$1\mu m$	Drain/Source Bottom Cap (C_j)	$660\mu F/m^2$
Gate Dielectric Thickness (t_{ox})	60\AA	Drain/Source Sidewall Cap (C_{jsw})	$4pF/m$
Base Threshold Voltage (V_{TH0})	$0.6V$	Channel Length Mod. Coeff. (λ)	$0.025V^{-1}$

Table PS1.I

- (a) Sketch the $I_D - V_{DS}$ characteristics for V_{DS} from 0 to 5V and $V_{GS} = 0.4V, 2V$ and 5V, assuming $V_{SB} = 0$.
- (b) Sketch the $I_D - V_{GS}$ characteristics for $V_{DS} = 3V$ as V_{GS} varies from 0 to 3V with $V_{SB} = 0, 0.6V$, and 1.2V.
- (c) Calculate all device capacitances, i.e. any capacitance between every two of the four terminals of the MOS transistor except the one between the gate and bulk, and draw circuit schematics assuming the transistor operates in the cut-off, saturation, and triode regions. The built-in potential between the source/drain regions and bulk is given as $\Psi_0 = 0.7V$. Also assume in cut-off: $V_{SB} = 0V, V_{DB} = 0V$; in saturation: $V_{SB} = 0V, V_{DB} = 1V$; in triode: $V_{SB} = 0V, V_{DB} = 0.1V$.

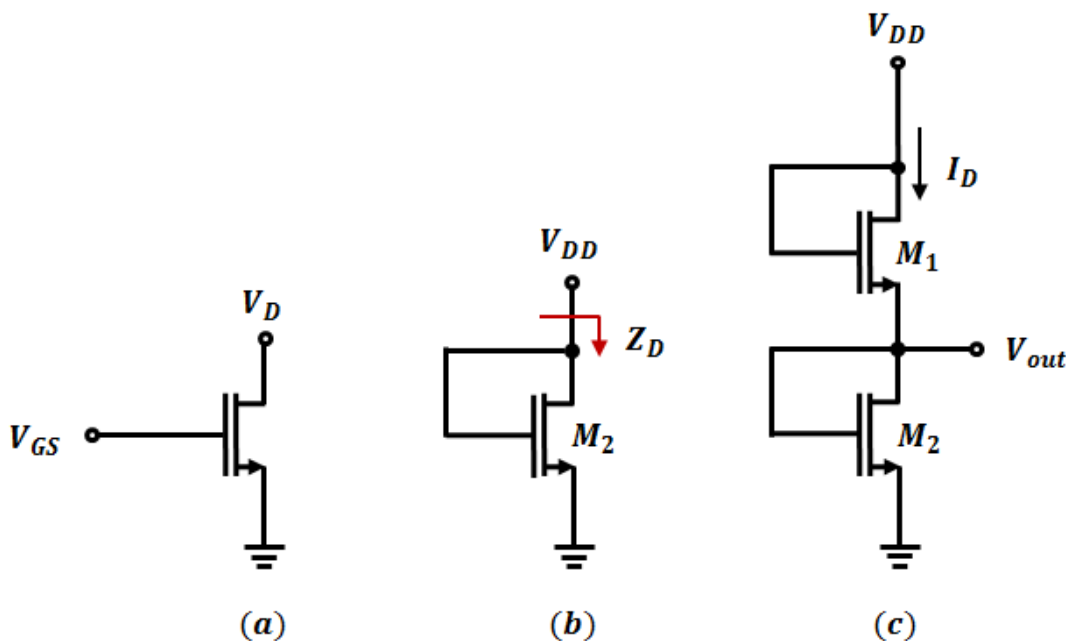


Fig. PS1.2

- (d) Assume the transistor is an n-channel enhancement type and hooked up to voltage sources as shown in Fig. PS1.2 (a). Sketch gate-to-drain (C_{GD}) and gate-to-source (C_{GS}) capacitances as gate-to-source (V_{GS}) voltage varies from 0V to infinity. Explicitly show and mark cut-off, saturation, and triode regions in your sketch. You can make any necessary assumptions to smoothen the transition between different operating regions.
- (e) Sketch the complete small-signal equivalent circuit for the device with $V_{GS} = 2V, V_{DS} = 4V$ and $V_{SB} = 0.8V$.
- (f) Under the bias condition in part (e), calculate the frequency of unity current gain of this device. Ignore the body effect.
- (g) The gate and drain terminals of the device are connected together as shown in Fig. PS1.2 (b). Determine in which region this transistor is operating and calculate the small-signal impedance (Z_D) indicated. Assume $V_{DD} = 5V$ and ignore the body effect.

(h) Now assume two identically connected transistors from part (g) are stacked together as shown in Fig. PS1.2 (c). If the width-to-length ratios of M_1 and M_2 are $(W/L)_1 = (W/L)_2 = 40$, determine V_{GS1} , V_{GS2} , V_{out} , and I_D . Ignore the channel length modulation and body effect.

(i) Repeat part (h) if width-to-length ratios are changed to $(W/L)_1 = 40$ and $(W/L)_2 = 15$.

2. Consider the following circuit schematics:

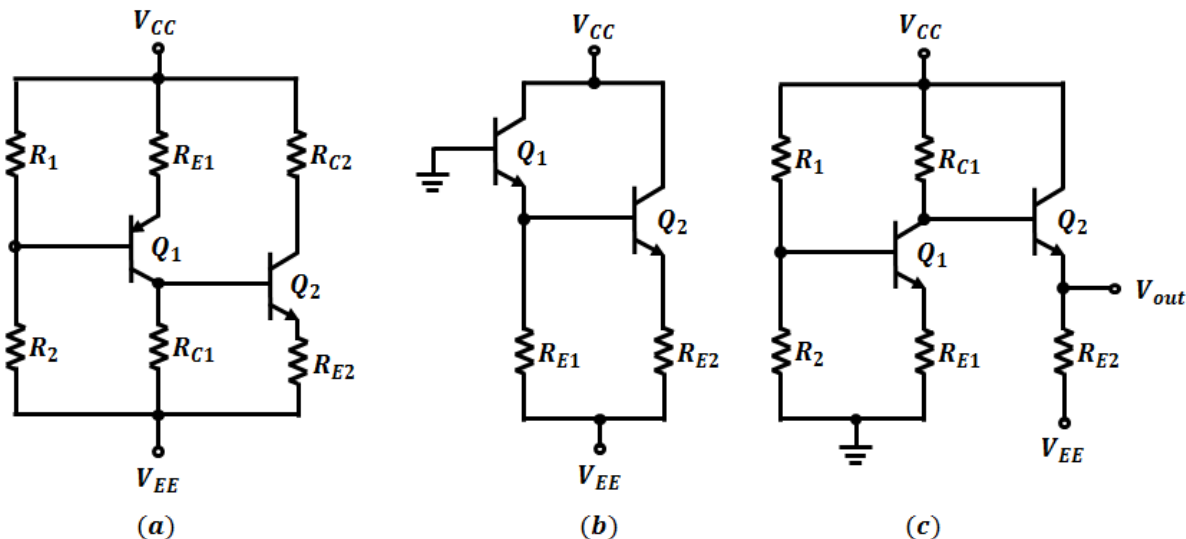


Fig. PS1.3

(a) For the circuit in Fig. PS1.3 (a) assume the transistor parameters are $\beta = 100$ and base-emitter junction turn-on voltage is $V_{BE} = 0.7V$. R_1 and R_2 are given as $50k\Omega$ and $100k\Omega$, respectively. Also the supply voltages are $V_{CC} = 5V$ and $V_{EE} = -5V$. Determine R_{C1} , R_{E1} , R_{C2} , and R_{E2} such that $I_{C1} = I_{C2} = 0.8mA$, $V_{ECQ1} = 3.5V$, and $V_{CEQ2} = 4.0V$.

(b) For the circuit in Fig. PS1.3 (b) assume the transistor parameters are $\beta = 80$ and base-emitter junction turn-on voltage is $V_{BE} = 0.7V$. R_{E1} and R_{E2} are given as $20k\Omega$ and $1k\Omega$, respectively. Also the supply voltages are $V_{CC} = 5V$ and $V_{EE} = -5V$. Determine the quiescent base, collector, and emitter currents in Q_1 and Q_2 . Also determine V_{CEQ1} and V_{CEQ2} .

(c) For the circuit in Fig. PS1.3 (c) assume the transistor parameters are $\beta = 120$ and base-emitter junction turn-on voltage is $V_{BE} = 0.7V$. Also $R_1 = 100k\Omega$, $R_2 = 40k\Omega$, $R_{C1} = 3k\Omega$, $R_{E1} = 1k\Omega$, and $R_{E2} = 5k\Omega$. The supply voltages are $V_{CC} = 10V$ and $V_{EE} = -10V$. Determine the quiescent base, collector, and emitter currents in Q_1 and Q_2 . Also determine V_{CEQ1} , V_{CEQ2} , and V_{out} .

3. An abrupt silicon pn junction is doped at $N_A = 10^{18} \text{ atoms/cm}^3$ (p-type) and $N_D = 10^{15} \text{ atoms/cm}^3$ (n-type).

- (a) Calculate the built-in potential, depletion layer depths, and maximum field for (i) $V_R = -0.2V$, (ii) $V_R = 1V$, and (iii) $V_R = 10V$.
- (b) Calculate the junction capacitance for (i) $V_R = -0.2V$, (ii) $V_R = 1V$, and (iii) $V_R = 10V$. Assume the junction area is 10^{-5} cm^2 .
- (c) An inductance of $2.2mH$ is placed in parallel with the pn junction. Calculate the resonance frequency, f_0 , of the circuit for (i) $V_R = -0.2V$, (ii) $V_R = 1V$, and (iii) $V_R = 10V$.