PROBLEM SET #10

Issued: Tuesday, Nov. 17, 2015

Due (at 8 a.m.): Wednesday, Nov. 25, 2015, in the EE 140/240A HW box near 125 Cory.

1. In the two stage op amp of Fig. PS10-1, $W/L_{1\text{-}4} = 50/0.5$. Also, $I_{SS} = 0.25$ mA, each output branch is biased at 1 mA, and $V_{DD} = 3$V. Use the parameters in the table below.

NMOS Model			
LEVEL = 1	VTO = 0.7V	GAMMA = 0.45	PHI = 0.9
NSUB = 9e+14	LD = 0.08μm	μ_n = 350cm^2/Vs	λ_n = 0.1 V$^{1/2}$
TOX = 9nm	PB = 0.9V	CJ = 0.56e-3 F/m^2	CJSW = 0.35e-11 F/m
MJ = 0.45	MJSW = 0.2	CGDO = 0.4e-9 F/m	JS = 1.0e-8 A/m^2
PMOS Model			
LEVEL = 1	VTO = -0.8V	GAMMA = 0.4	PHI = 0.9
NSUB = 5e+14	LD = 0.09μm	μ_p = 100cm^2/Vs	λ_p = 0.2 V$^{1/2}$
TOX = 9nm	PB = 0.9V	CJ = 0.94e-3 F/m^2	CJSW = 0.32e-11 F/m
MJ = 0.5	MJSW = 0.3	CGDO = 0.3e-9 F/m	JS = 0.5e-8 A/m^2

(a) If a maximum output swing from 0.4-2.4V is desired, design $W/L_{5\text{-}8}$.

(b) Determine the CM level at nodes X and Y with $W/L_{5.6} = 60/0.5$ and $W/L_{7.8} = 50/0.5$.Use these sizes for the rest of this problem.

(c) If each output is loaded by a 1-pF capacitor, compensate the op amp using Miller capacitors C_C connected from the gates to the drains of $M_{5.6}$ to achieve a phase margin of 60^o in unity-gain feedback. Calculate the pole and zero positions after compensation.

(d) Design the resistance that must be placed in series with the compensation capacitors to position the zero atop the non-dominant pole.

(e) Determine the slew rate.

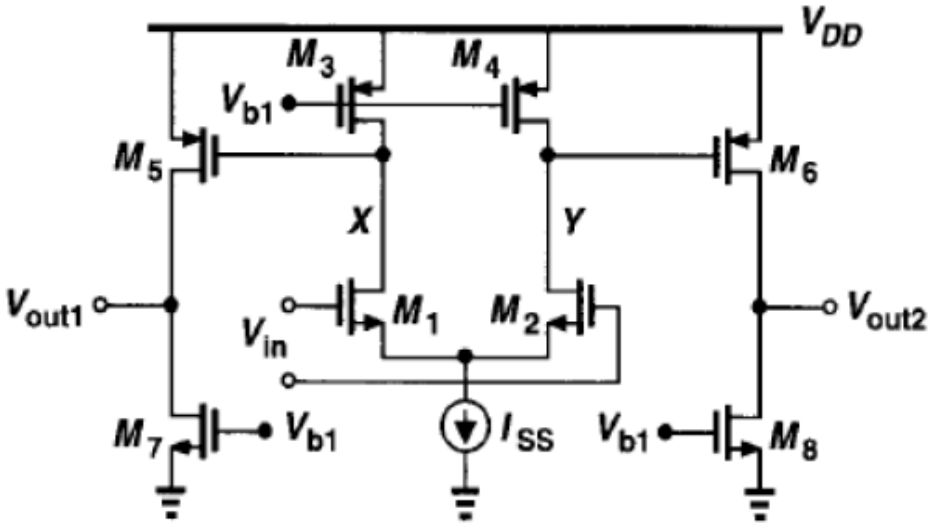

Fig. PS10-1

2. In this problem, you will simulate using Hspice the op amp given in "ee140_hw10.sp." Its accompanying device model is given in "ee140_hw10_model.sp." For your convenience, the op amp circuit is pictorially shown below in Fig. PS10-2. Please give all gain values and ratios in dB.

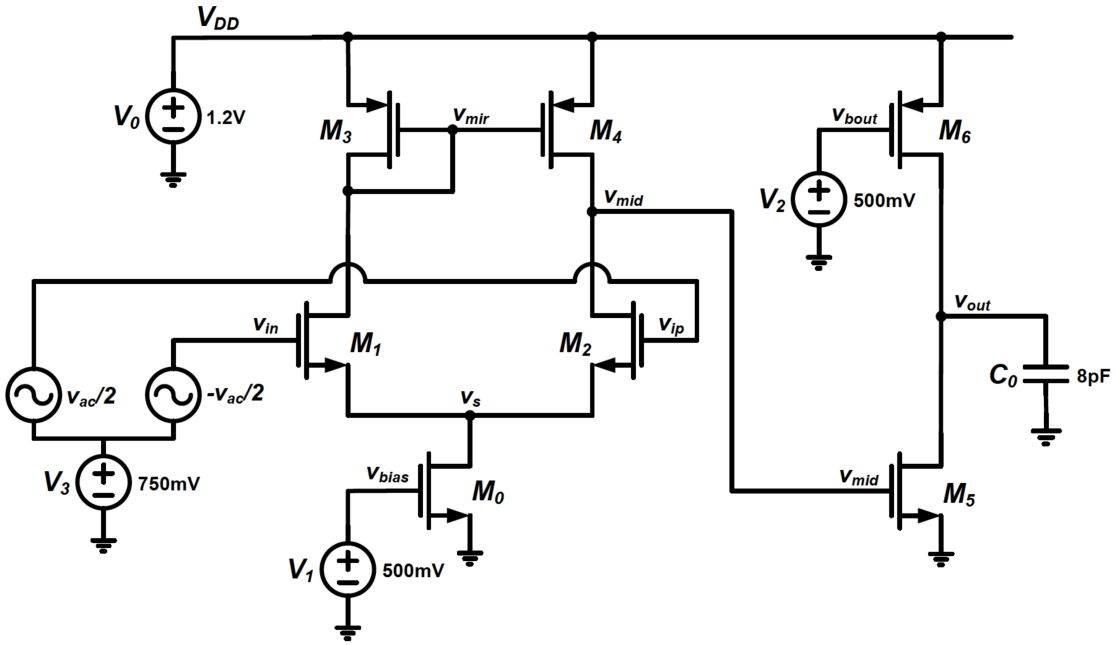

Fig. PS10-2

(a) Simulate the open loop AC gain and phase of the op amp. What is the op amp's gain at low frequencies? What is the op amp's unity gain frequency? What is the op amp's unity gain phase margin?

(b) Simulate the common mode gain of the op amp by applying positive v_{ac} voltages to both inputs. What is the op amp's common mode gain at low frequencies? What is the op amp's CMRR?

(c) Simulate the power supply gain of the op amp by turning off the AC signal at the op amp's inputs and adding an AC signal to the power supply voltage source V_{DD}. What is the op amp's power supply gain at low frequencies? What is the op amp's PSRR?

(d) Simulate the output swing of the op amp using a DC sweep analysis:

i. Sweep the DC voltage at one of the op amp's inputs around its bias point.

ii. Take the derivative of the op amp's DC output voltage with respect to the swept input.

Make sure there is enough resolution in your sweep to get an accurate result.

For the purpose of this course (and your project), we will define the op amp's output swing range as the DC output voltages at which dV_{out}/dV_{in} becomes 1/10 the nominal differential gain (from part (a)). What is the op amp's output swing range?

(e) Simulate the common mode input range of the op amp using DC sweep analysis:

i. Put the op amp into unity gain feedback.

ii. Sweep the DC voltage of the op amp's input from 0 to V_{DD}.

iii. Take the derivative of the op amp's DC output voltage with respect to the swept input.

For the purpose of this course (and your project), we will define the op amp's input range as the DC input voltages at which dV_{out}/dV_{in} becomes 1/2 in unity gain feedback. What is the op amp's common mode input range?