PROBLEM SET #4

Issued: Tuesday, Sep. 22, 2015

Due (at 8 a.m.): Wednesday, Sep. 30, 2015, in the EE 140/240A HW box near 125 Cory.

1. This problem considers non-ideality current mirrors formed using BJT pairs. In Fig. PS4-1(a), assume Q_2 has m times the area of Q_1, i.e., $I_{S2} = m \times I_{s1}$. Ignore Early effect.

(a) Assuming $\beta = \infty$, show that $I_{out} = m \times I_{ref}$

(b) Assuming β is finite, find the expression of I_{out} in terms of I_{ref}, β, and m.

(c) The error introduced by the finite β effect takes the form $1 - I_{out(b)} / I_{out(a)}$. Assume $\beta = 80$, what is the largest m such that the error is smaller than 5%?

(d) Fig. PS4-1(b) presents a circuit that reduces the error in part (c). Assuming all transistors have the same area and β, find the expression for I_{out} in terms of I_{ref} and β.

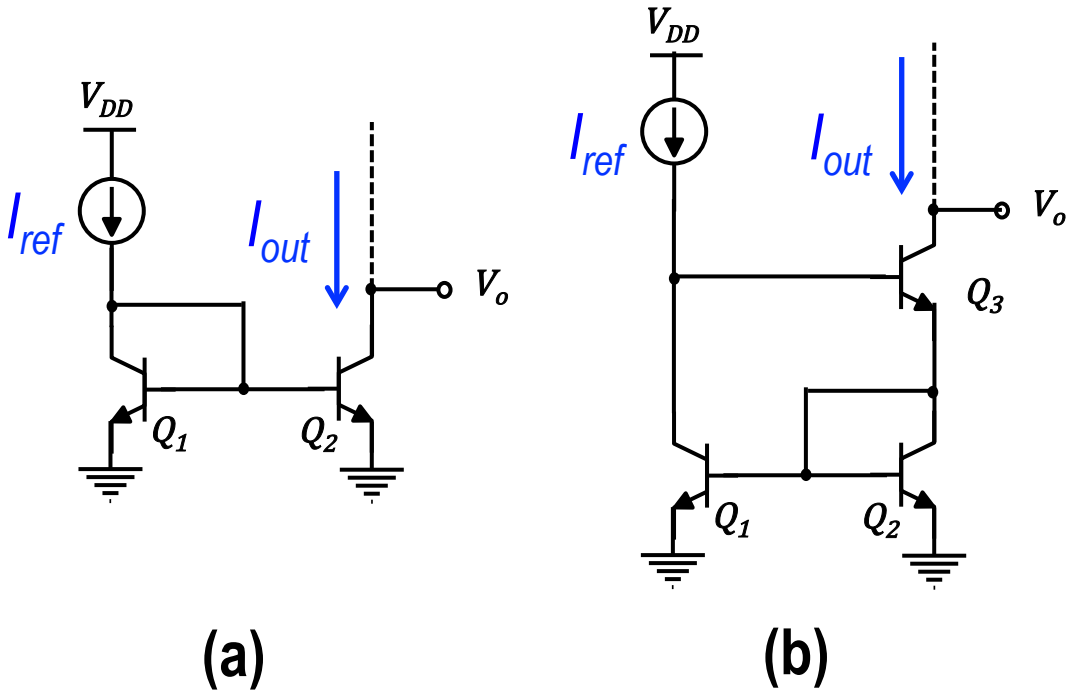

Fig. PS4-1

2. Fig. PS4-2 shows a bias-network designed for circuit blocks A and B using transistors with $\mu_n C_{ox} = 200\mu A/V^2$, $\mu_p C_{ox} = 80\mu A/V^2$, $V_{tn} = 0.6V$, $V_{tp} = -0.6V$, and where all transistor lengths are $L = 0.8\mu m$. Ignore channel-length modulation. Design all transistor widths and R to fulfill the following specifications:

(a) $I_{REF} = I_{REF2} = 20\mu A$.

(b) During operation, circuit block A consumes $100\mu A$, and V_A can vary from 0 to 1.3V.

(c) During operation, circuit block B consumes $50\mu A$, and V_B could vary from -1.3V to 1.3V.

(d) Minimize the overall circuit area. In other words, use the minimum possible device widths to fulfill the requirements.

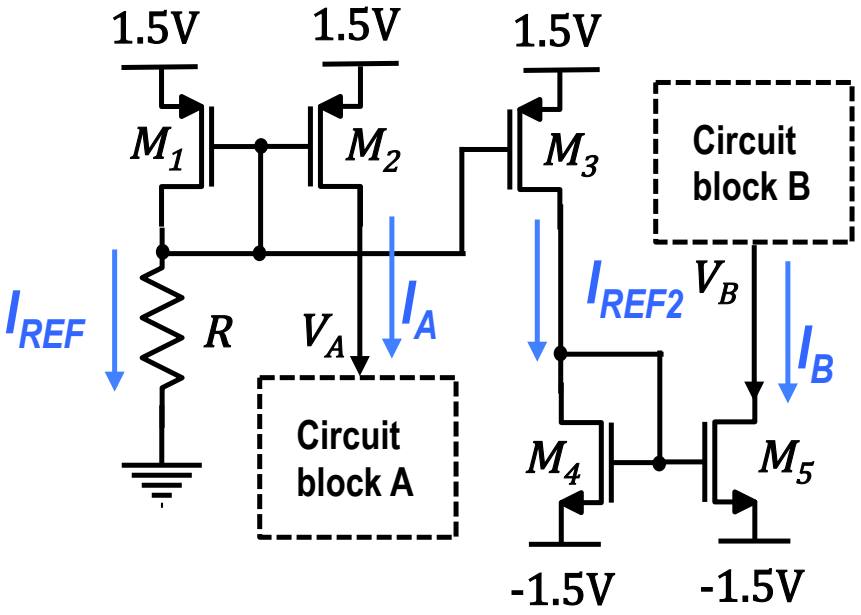

Fig. PS4-2

3. For the transistors in the amplifier shown in Fig. PS4-3, $\mu_n C_{ox} = 800\mu\text{A/V}^2$, $\mu_p C_{ox} = 400\mu\text{A/V}^2$, $V_{tn} = 0.8\text{V}$, $V_{tp} = -0.8\text{V}$, and $\lambda_n = \lambda_p = 0.05\text{V}^{-1}$. The signal source V_{sig} is a small sinusoidal signal with no DC component.

(a) Neglecting channel-length modulation, design the value of V_{bias} such that the output swing is maximized.

(b) Find the midband voltage gain V_o/V_{sig}, R_{in}, and R_{out}.

(c) How large can V_{sig} swing (peak-to-peak) while M_1 and M_2 stay in saturation?

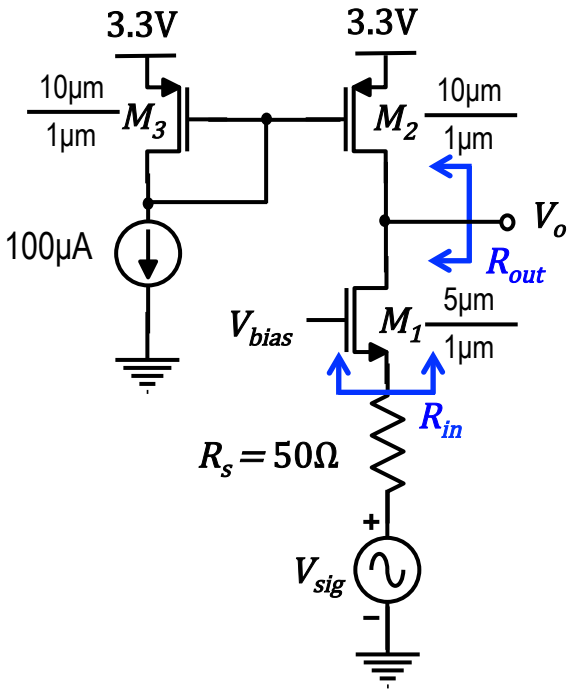

Fig. PS4-3

4. Consider the BiCMOS amplifier shown in fig. PS4-4(a). The BJT has $|V_{BE}| = 0.7$V, β =200, C_μ = 0.8pF, and f_T = 600MHz. The NMOS transistor has V_t = 1V, $\mu_n C_{ox} W/L = 2\text{mA/V}^2$, C_{gs} = 2pF, and C_{gd} = 1pF. The large feedback resistor R_G helps with biasing, among other purposes. This problem considers the effect of R_G.

(a) Find the dc bias current for M_1 and Q_2.

(b) Assuming $R_G = \infty$, find the midband voltage gain V_o/V_{sig} , R_{in} , and ω_H of the circuit. You can neglect C_{sb} and C_{db}.

(c) Redo part (b) with $R_G = 10\text{M}\Omega$. Apply Miller theorem on R_G. How does R_G affect V_o/V_{sig}, R_{in}, and ω_H?

(d) To mitigate the effect of R_G one could cut R_G into 2 segments and insert a large capacitor between them as in Fig. PS4-4(b). Redo part (c) with R_G replaced with this new feedback network.

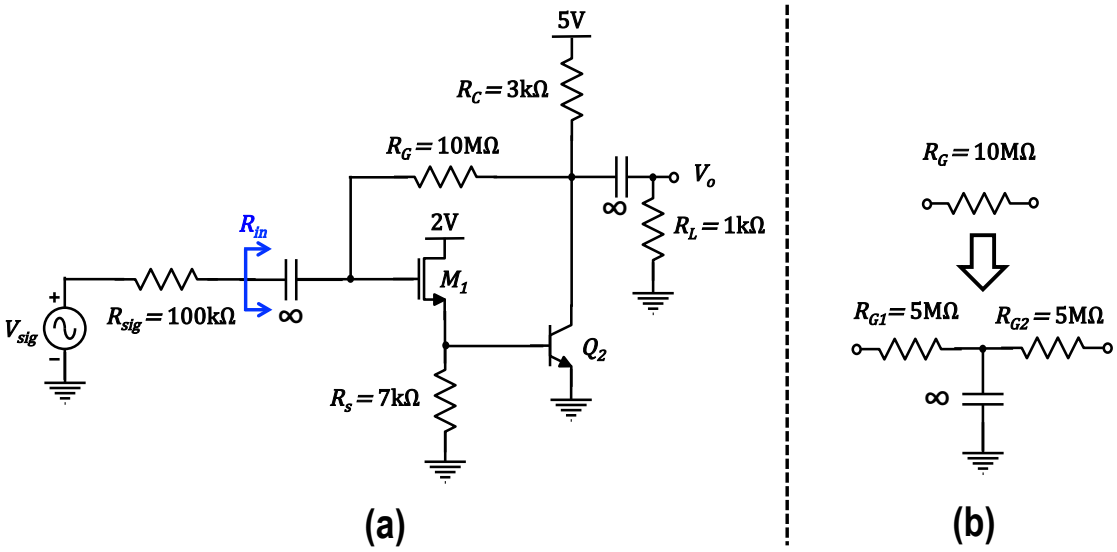

Fig. PS4-4