PROBLEM SET #7

Issued: Friday, Oct. 16, 2015

Due (at 8 a.m.): Monday, Oct. 26, 2015, in the EE 140/240A HW box near 125 Cory.

- 1. A design error has resulted in a mismatch in the circuit of Fig. PS7-1. Specifically, M_2 has twice the W/L ratio of M_1 . If V_{id} is a small sine-wave signal, find an expression for
 - (a) I_{D1} and I_{D2} .
 - (b) V_{OV} for each of M_1 and M_2 .
 - (c) The differential gain A_{dm} in terms of R_D , I, and V_{OV} .

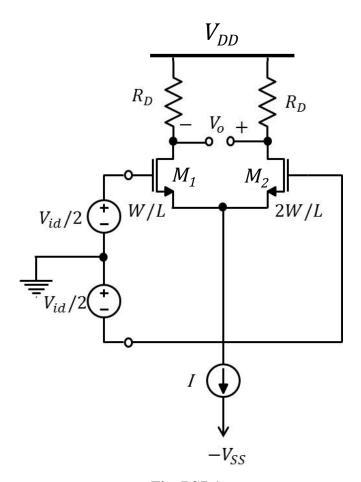


Fig. PS7-1

- 2. The differential amplifier in Fig. PS7-2 utilizes a resistor R_{SS} to establish a 1-mA dc bias current. Note that this amplifier uses a single 5-V supply and thus needs a dc common-mode voltage V_{CM} . Transistors M_1 and M_2 have $k'W/L = 2.5 \text{mA/V}^2$, $V_t = 0.7 \text{V}$, and $\lambda = 0$.
 - (a) Find the required value of V_{CM} .
 - (b) Find the value of R_D that results in a differential gain A_{dm} of 8 V/V.
 - (c) Determine the dc voltage at the drains
 - (d) Determine the common-mode gain v_D/v_{CM} and CMRR for this amplifier. (Hint: You need to take $1/g_{\rm m}$ into account.)
 - (e) Use the common-mode gain found in (d) to determine the change in V_{CM} that results in M_1 and M_2 entering the triode region.

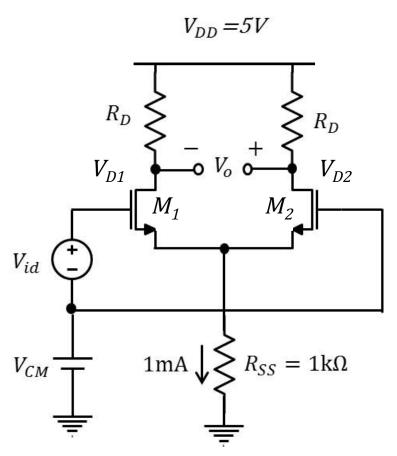


Fig. PS7-2

3. Fig. PS7-3 shows a high-gain op amp design with cascade devices. Let $I_{SS} = 1$ mA, $V_{DD} = 3$ V, $V_{B1} = 1.7$ V and $V_{B2} = 1.6$ V. Assuming $\gamma = 0$ and $V_{ov,Iss} = 0.2$ V, find the mid-band gain v_{out}/v_{in} , input common-mode range, and the output swing.

MOS Parameters:

$$\mu_n C_{ox} = \frac{135 \mu A}{V^2}, \mu_p C_{ox} = \frac{38 \mu A}{V^2} V_{Tn} = 0.7 \text{ V}, V_{Tp} = -0.8 \text{ V}, \lambda_n = \lambda_p = 0.1,$$

$$\left(\frac{W}{L}\right)_{1,2,3,4} = \frac{100 \mu m}{0.34 \mu m}, \left(\frac{W}{L}\right)_{5,6,7,8} = \frac{100 \mu m}{0.32 \mu m}$$

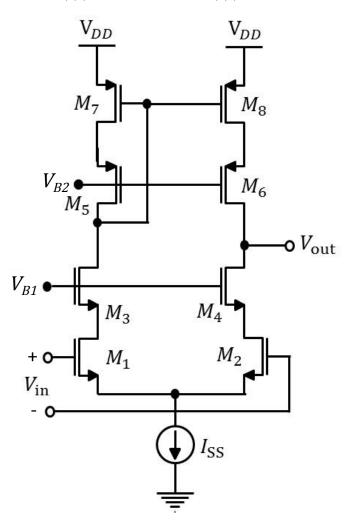


Fig. PS7-3

4. Fig. PS7-4 shows a two-stage CMOS op amp. Let $I_{REF} = 90 \mu A$, $V_{DD} = V_{SS} = 2.5 V$, and $C_C = 0$. Find the mid-band gain $v_O/(v_+ - v_-)$, input common-mode range, and the output swing.

MOS Parameters:

$$\begin{split} \mu_n C_{ox} &= \frac{160 \, \text{µA}}{\text{V}^2} \text{,} \\ \mu_p C_{ox} &= \frac{40 \, \text{µA}}{\text{V}^2} \text{ ,} \\ V_{Tn} &= 0.7 \text{ V} \text{,} \\ V_{Tp} &= -0.8 \text{ V} \text{,} \\ \lambda_n &= \lambda_p = 0.1 \text{,} \\ \left(\frac{W}{L}\right)_{1,2} &= \frac{20 \, \text{µm}}{0.8 \, \text{µm}} \text{,} \\ \left(\frac{W}{L}\right)_{3,4} &= \frac{5 \, \text{µm}}{0.8 \, \text{µm}} \text{,} \\ \left(\frac{W}{L}\right)_{5,7,8} &= \frac{40 \, \text{µm}}{0.8 \, \text{µm}} \text{,} \\ \left(\frac{W}{L}\right)_{6} &= \frac{10 \, \text{µm}}{0.8 \, \text{µm}} \end{split}$$

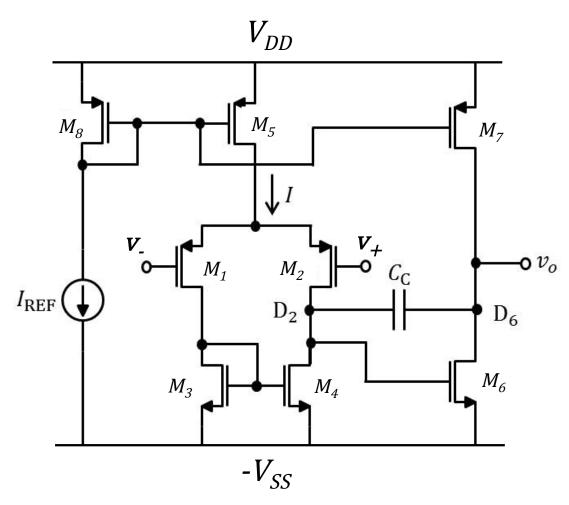


Fig. PS7-4

- **5.** Fig. PS7-5 shows a multi-stage BJT OPAmp design. BJTs $Q_1 Q_9$ have the same size except for Q_6 , which is 4x larger than Q_9 . Ignore Early effect.
 - (a) Assuming $\beta \gg 1$ and $|V_{BE}| = 0.7V$, calculate the DC currents flowing through $Q_1 Q_9$.
 - (b) Calculate the static power dissipation of this op amp.
 - (c) If transistors Q_1 and Q_2 have $\beta = 100$, what is the input bias current of this op amp?
 - (d) If $V_{CE(sat)} = 0.4$ V, determine the input common-mode range of this op amp.
 - (e) Calculate the input resistance, mid-band gain v_o/v_{id} , and the output resistance of this op amp.

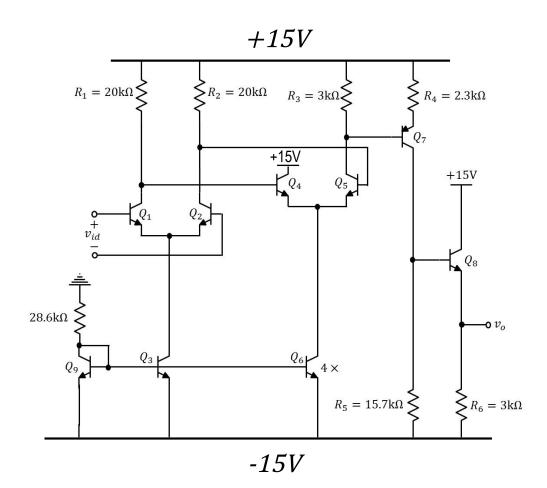


Fig. PS7-5