INFORMATION ABOUT THE MIDTERM EXAM

Extra Office Hours: (in addition to regular office hours, of which there are plenty)

Prof. Nguyen 2:30-4:00 p.m. on Wednesday, March 18

Date of Exam:

Thursday, March 19, 12:30-2 p.m. (sharp)

Place:

101 Moffitt (our regular room)

General Information:

The exam will be closed book, but you will be allowed one sheet on which you can write anything you would like. Bring a calculator to the exam. You will be provided with exam sheets with enough space to put all your work on these sheets. You should show and include all your work on the exam sheets. The exam will consist of a few problems, each with a number of parts.

During the exam, make appropriate engineering decisions and approximations in order to simplify your analyses so that you can do the problems quickly and with fewer errors. In other words, the use of inspection analysis (where applicable) is encouraged.

Material to be Covered:

Reading in Razavi, class lecture notes, handouts, and homeworks. The exam is meant to include all material covered so far in the class. You might pay more attention to the following areas:

1. Bipolar and MOS small-signal model generation and analysis.
2. Single and multiple transistor amplifier circuits, using BJT and/or MOS transistors, including cascodes and cascades, either actively or passively loaded. Be able to determine bias points, gain, impedance, and frequency response.
3. Differential pair amplifiers, either actively or passively loaded, including such concepts as biasing, differential-mode gain, common-mode gain, CMRR, half-circuits, and various impedances.
4. Derivation of input offset voltages for (possibly unfamiliar) circuits.
5. Transistor bias generators and current sources, including ability to determine output current, output resistance, and output swing for a circuit using a given (possibly unfamiliar) current source. You should also be able to design a current source to insure a given swing for a given biased amplifier circuit.
6. Biasing and small-signal analysis (for gain, impedance, and dominant pole) of single and two-stage op amps.
7. Analysis and evaluation of circuits using op amps with finite gain, finite bandwidth, and/or input offset voltages.