

**Laboratory 1**  
**Single-Stage MOSFET Amplifier Analysis and Design**  
**Due Date: Week of February 23, 2009, at the beginning of your lab section**

**Objective**

To analyze and design single-stage common source amplifiers. This lab does not require the building of the circuit because we do not have access to appropriate transistors. Design objectives can be accomplished and verified using hand calculations and SPICE simulations.

**Introduction:**

Since MOS technology is playing a more central role in today's analog integrated circuits, it is important to have a good understanding of MOS transistor amplifier analysis and design. It is the goal of this lab to enable you to understand the inter-relationships among gain, bandwidth, device dimensions and bias point specifications for MOS amplifiers through a simple design. Most of the knowledge obtained in this lab will be used in the design project later this semester. In the first lab you are asked to analyze, design, and simulate a simple MOS amplifier to satisfy a given set of specifications.

**Part 1:**

In this first part you will analyze and simulate a saturated NMOS load common-source amplifier shown in Figure 1 below.

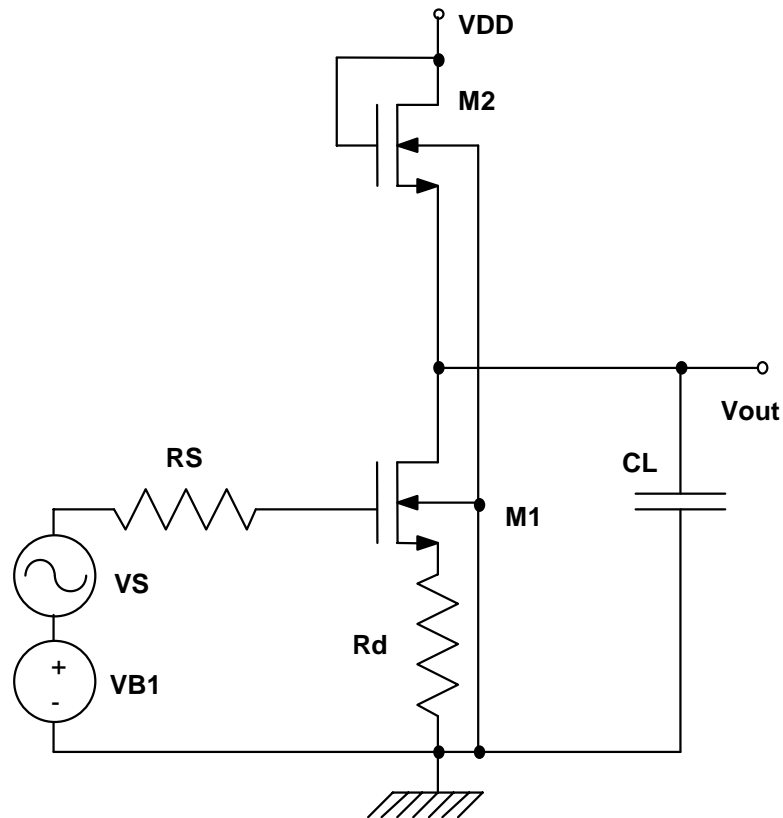


Figure 1: Saturated NMOS Load common-source amplifier.

There are two tasks in this part. For both parts assume the following parameters for the transistor when doing hand calculations and SPICE simulations:

***PROCESS/SPICE PARAMETERS FOR NMOS/PMOS TRANSISTORS***

<i>Parameter</i>	<i>NMOS</i>	<i>PMOS</i>
Level	4 (In HSPICE)	4 (In HSPICE)
VTO	0.8 V	-0.8 V
KP	$90 \mu\text{A}/\text{V}^2$	$30 \mu\text{A}/\text{V}^2$
GAMMA	$0.8 \sqrt{V}$	$0.4 \sqrt{V}$
LAMBDA	$0.01 \text{ V}^{-1}$	$0.02 \text{ V}^{-1}$
TOX	200 Å	200 Å
XJ	0.5 $\mu\text{m}$	0.5 $\mu\text{m}$
LD	0.3 $\mu\text{m}$	0.3 $\mu\text{m}$
PHI	0.7 V	0.6 V
NSUB	$3.33 \times 10^{16} \text{ cm}^{-3}$	$3.33 \times 10^{15} \text{ cm}^{-3}$
RSH	0 $\Omega$	0 $\Omega$
CGSO	500P, F/M	500P, F/M
CGDO	500P, F/M	500P, F/M
CGBO	0, F/M	0, F/M
CJ	300U, F/M <sup>2</sup>	300U, F/M <sup>2</sup>
MJ	0.5	0.5
CJSW	0, F/M	0, F/M
MJSW	0.33	0.33

Note that all biasing in this circuit is performed using the DC source VB1. The power supply for this amplifier is  $V_{DD} = 5\text{V}$ . There are two external elements in this amplifier:

$$R_S = \text{Source Resistance} = 1\text{M}\Omega$$

$$C_L = \text{Load Capacitance} = 5\text{pF}$$

$$R_d = \text{Degeneration Resistance (Will Be Given Later)}$$

**Task a:**

Assume that:

$$V_{B1} = 1.1\text{V}$$

$$R_d = 0 \text{ (i.e. no degeneration)}$$

$$(W/L)_1 = (40/5) \mu\text{m}/\mu\text{m}$$

$$(W/L)_2 = (5/90) \mu\text{m}/\mu\text{m}$$

Determine the small-signal voltage gain  $v_o/v_s$ , the upper cutoff frequency (or bandwidth), and the output resistance of the amplifier using BOTH hand calculation and SPICE simulation. You should show the plot of the magnitude of the gain in dB vs.  $\log(\text{frequency})$  for

this amplifier. Note that you can make any reasonable approximations in your hand calculations. If the simulated and calculated results do not agree you should discuss the reasons. Also determine the maximum output voltage swing that this amplifier can deliver. You can use SPICE simulation only for this part.

**Task b:**

In this part we add some degeneracy into the circuit by changing the value of resistor  $R_d$ . You can assume that:

$$V_{B1} = 1.3V$$

$$R_d = 5k\Omega$$

$$(W/L)_1 = (40/5) \mu\text{m}/\mu\text{m}$$

$$(W/L)_2 = (5/90) \mu\text{m}/\mu\text{m}$$

Determine the small-signal voltage gain  $v_o/v_s$ , the upper cutoff frequency (or bandwidth), and the output resistance of the amplifier using BOTH hand calculation and SPICE simulation. You should show the plot of the magnitude of the gain in dB vs.  $\log(\text{frequency})$  for this amplifier. Note that you can make any reasonable approximations in your hand calculations. If the simulated and calculated results do not agree you should discuss the reasons. Also determine the maximum output voltage swing that this amplifier can deliver. You can use SPICE simulation only for this part.

For both of these tasks you should list the relevant performance parameters in a Table.

**Part 2: MOS Amplifier Design:**

In this part you are asked to design a common-source amplifier with a saturated PMOS load as shown in the figure below:

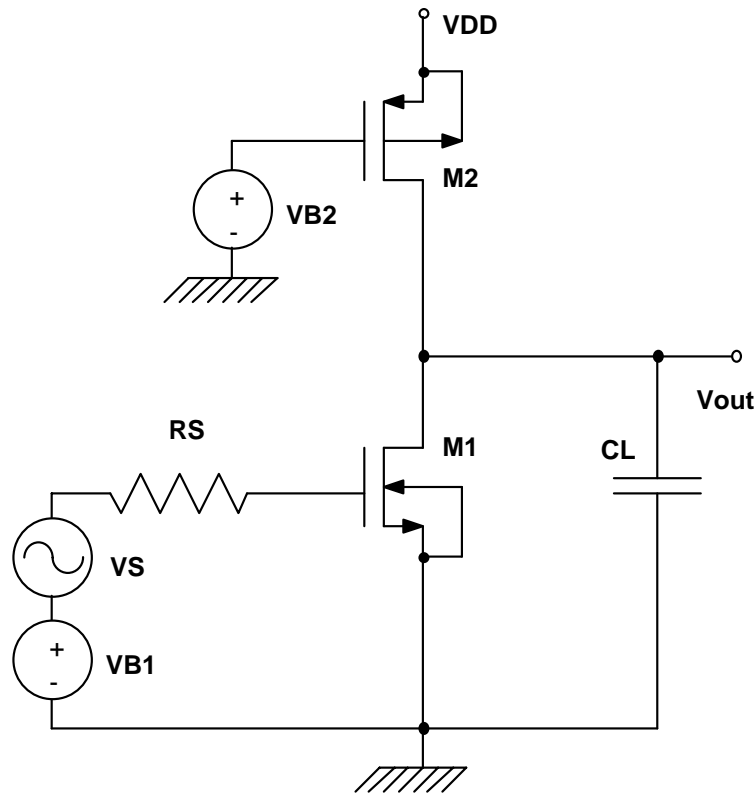


Figure 2: Common-source amplifier with a PMOS saturated load.

Note that all biasing in this circuit is performed with two DC sources VB1 and VB2. The power supply for this amplifier is  $V_{DD} = 5V$ . In your design you have to determine the values of these two sources. There are two external elements in this amplifier:

$$R_S = \text{Source Resistance} = 2M\Omega$$

$$C_L = \text{Load Capacitance} = 2pF$$

Design the above common-source amplifier so that it satisfies the following specifications:

<i>Parameter</i>	<i>Specification</i>
Midband Gain	$\geq 120$ V/V
3dB Cutoff Frequency	$\geq 20$ kHz
Output Voltage Swing	Within 0.5V of VDD & Ground
Load Capacitance, CL	2pF
Source Resistance, RS	2 M $\Omega$
Supply Voltage:	$V_{DD} = +5V, V_{SS} = \text{Ground} = 0V$

There are several important issues that you have to remember as you design your amplifier. These are itemized below:

1. Note that the Lambda value is given for  $L=5\mu\text{m}$ . All of your transistors should have a length of  $5\mu\text{m}$ . You cannot use any other channel length for this problem. For Lambda calculation you can ignore lateral diffusion and assume that the value of Lambda at  $L=4.4\mu\text{m}$  is the same as that at  $L=5\mu\text{m}$ .
2. The gate oxide thickness is provided so that you can calculate the relevant capacitances that you need in your calculations. Note that some of the capacitance parameters that are typically needed in SPICE are already calculated for you. You may need some of these in your design.
3. When you perform the design you should ensure that the circuit is biased such that all transistors are in saturation. This may require very fine tuning of the bias voltages VB1 and VB2 down to the millivolt value. The reason for this is that the amplifier has such a high gain that the slightest shift in the bias point value will cause one or the other transistor to come out of saturation.
4. When biasing these transistors you should not use a  $V_{GS} - V_T$  of smaller than 200mV for either of the transistors. This means that the  $V_{GS}$  across either transistor has to be higher than 1.0V.

You should pay attention to the following in your design:

1. You need to determine the dimensions for both transistors M1 and M2, as well as the values for bias sources VB1 and VB2 at the end of your design. In addition, you should show both by hand calculations and computer simulations that the specifications have been satisfied. Include plots (or tables) of simulations results where necessary and make sure that all plots are labeled appropriately. The hand calculations and the equations and relationships you use are very important and they should be included in your lab report. All equations should be in variable form before numerical evaluation. Your design approach should be outlined in your report. Your hand calculations and simulation results may differ quite significantly. Try to explain why this is the case if you observe this.
2. Calculate the output resistance of the final amplifier and compare it with the output resistance of the CS amplifier used in Task a of Part 1.
3. You should use HSPICE, Level=4, for this lab.
4. You are to work on this lab individually. Although you can discuss generalities with other students in the class, you are not to perform the design in teams or groups.
5. Your lab report should be brief, concise, and complete, and should include your hand calculations, and a table comparing the design specifications as well as your actual circuit's specifications. A discussion on the tradeoffs and design strategy should be provided in your report. The report need not be very long, and the format of the report is left up to you. Just make sure that the report is clear and easy to read so that your TA can follow your

presentation. If you cannot meet the design specifications make sure that your report states why and explain what critical factors prevented you from achieving your design goals and suggest directions for modifying your design to meet specifications.

You should try your best to achieve the design specifications. If after all attempts you fail to meet all the design specifications, describe to us your final design and what you consider to have been the most restrictive and problematic spec to meet.