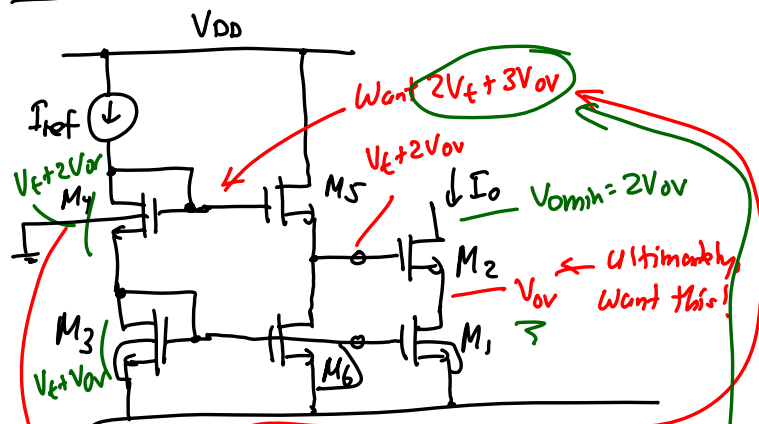


Today:

- High Swing Current Sources
- Current Source Matching Considerations
- Start Op Amps

Last Time -



To get this, must size M_4 accordingly:

$$I_{D3} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_3 (V_{ov3})^2$$

$$I_{D4} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_4 (2V_{ov3})^2$$

$$V_{ov4} = 2V_{ov3}$$

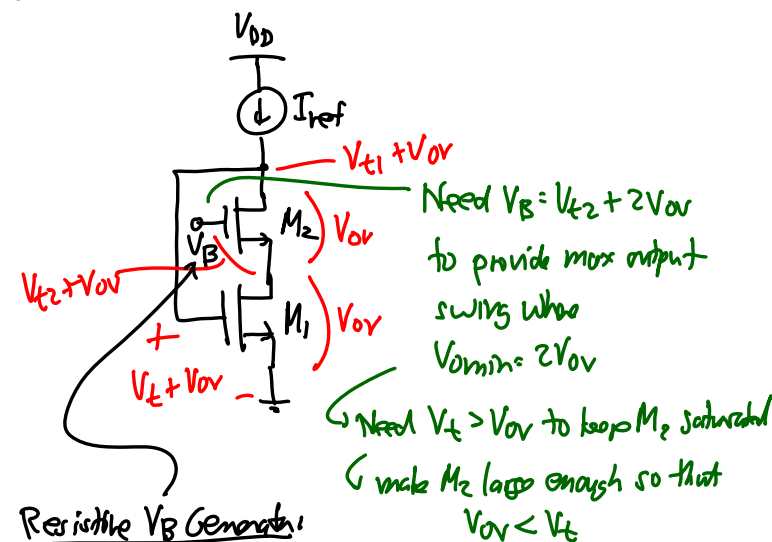
$$I_{D3} = I_{D4} = I_{ref}$$

$$\frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_3 (V_{ov3})^2 = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right)_4 (2V_{ov3})^2$$

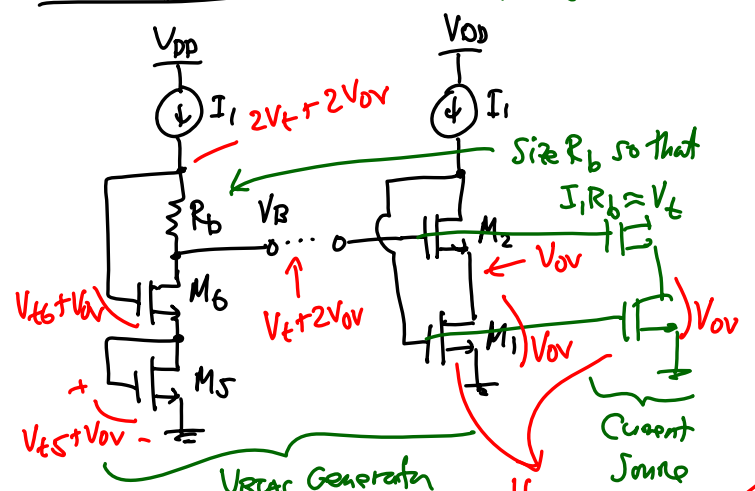
$$\left(\frac{W}{L}\right)_4 = \frac{1}{4} \left(\frac{W}{L}\right)_3$$

$$\dots \text{and } \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_5 = \left(\frac{W}{L}\right)_6 \quad \checkmark$$

Alternate Biasing Scheme for Cascode



Revisit the V_B Generator:



Issues:

- ① $I_1 R_b$ not all that well-controlled.
- ② Must still account for Body Effect.
↳ so really need: $I_1 R_b = V_{t5} + V_{t6} - V_{t2}$

Replace R_b w/ a transistor level-shift:

Design: (for now, ignore Body effect) insist that all devices are saturated

Approach 1: Want $V_{GS7} = V_t$ want $V_{DS6} = V_{ov} \rightarrow$ need $V_{GS7} = V_t$

Normally, $V_{GS7} = V_t + V_{ov}$

can make $V_{ov} \approx 0V$, if make M_7 huge! $\Rightarrow (\frac{W}{L})_7 = \text{large}$

takes up chip area

problem! (will cost too much)

$V_{ov7} = \sqrt{\frac{2I_D}{\mu_n C_{ox} (\frac{W}{L})_7}}$

Approach 2: \rightarrow recognize that devices in the

- Allow M_7 to drop $V_{GS7} = V_t + V_{ov}$. V_{DS7} - generate need NOT be saturated
- Still need $V_{DS6} = V_{DS7} = V_{ov7}$
- Can get this by operating M_6 in the triode region.

too much voltage!
 $\rightarrow 2V_t + 2V_{ov} \approx 2(0.7) + 2(0.3) = 1.4 + 0.6 = 2V$
 some can be in triode!
 too much in 2V supply!

M_7 saturated: $I_{D7} = \frac{1}{2} \mu_n C_{ox} (\frac{W}{L})_7 (V_{GS7} - V_t)^2$

M_6 linear (or triode): $I_{D6} = \frac{1}{2} \mu_n C_{ox} (\frac{W}{L})_6 [2(V_{GS6} - V_t)V_{DS6} - V_{DS6}^2]$

Want: when $V_{GS7} = V_t + V_{ov7} \rightarrow$ want $V_{DS6} = V_{ov7}$

Thus: $I_{D7} = I_{D6}$

$\frac{1}{2} \mu_n C_{ox} (\frac{W}{L})_7 (V_{ov7})^2 = \frac{1}{2} \mu_n C_{ox} (\frac{W}{L})_6 [2(2V_{ov7})V_{ov7} - (V_{ov7})^2]$

$(\frac{W}{L})_7 = 3(\frac{W}{L})_6$

$(\frac{W}{L})_6 = \frac{1}{3}(\frac{W}{L})_7$ & all other $\frac{W}{L}'s = (\frac{W}{L})_7$

Problem: We're using too much voltage to do this!

The diagram shows a differential pair of NMOS transistors, M_3 and M_4 , with their gates tied together and biased at $V_{gs} + 2V_{ov}$. The sources are connected to ground through NMOS transistors M_1 and M_7 . The drains are connected to V_{DD} through PMOS transistors M_2 and M_4 . Current sources I_1 and I_2 are connected to the gates and drains of M_3 and M_4 respectively. Handwritten notes indicate $V_{DD} = 2V_{ov}$ and $V_{gs} + 2V_{ov}$ for the gate biasing.

$$\frac{1}{2} \cancel{\mu_0} \cancel{\epsilon_0} \left(\frac{w}{\cancel{L}} \right)^2 (2V_{\cancel{DVS}})^2 = \frac{1}{2} \cancel{\mu_0} \cancel{\epsilon_0} \left(\frac{w}{\cancel{L}} \right)^2 (V_{\cancel{DVS}})^2$$

$$\therefore \left(\frac{w}{L} \right)_7 = \frac{1}{4} \left(\frac{w}{L} \right)_3 - \frac{1}{4} \left(\frac{w}{L} \right)$$

↑
all the Kristas
except M_7

↳ must design defensively...

↳ Marke $V_{GS7} > V_t + 2V_{OV3}$

Try to make $(\frac{W}{L})_1 = (\frac{W}{L})_2 \dots$ but
don't always get this.

In MOS, we often need matched current sources: $I_{O1} = I_{O2}$

$$I_{O1} = I_{D1} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_1 (V_{GS1} - V_{t1})^2$$

$$I_{O2} = I_{D2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_2 (V_{GS2} - V_{t2})^2$$

due to finite fabrication tolerances...

These won't be perfectly matched if $(w/l)_1 \neq (w/l)_2$ & $V_{t1} \neq V_{t2}$

To quantify this: Define average & mismatch quantities.

Average

$$I_D = \frac{1}{2} [I_{D1} + I_{D2}]$$

$$\frac{W}{L} = \frac{1}{2} \left[\left(\frac{W}{L} \right)_1 + \left(\frac{W}{L} \right)_2 \right]$$

$$V_f = \frac{1}{2} [V_{t1} + V_{t2}]$$

Mismatch

$$\Delta I_D = I_{D1} - I_{D2}$$

$$\Delta\left(\frac{w}{L}\right) = \left(\frac{w}{L}\right)_1 - \left(\frac{w}{L}\right)_2$$

$$\Delta V_t = V_{t1} - V_{t2}$$

$$\frac{\Delta I_D}{I_D} \triangleq \text{fractional current mismatch}$$

$$\frac{\Delta(w/l)}{(w/l)} = \text{fractional (w/l) mismatch}$$

$$\frac{\Delta V_b}{V_t} \approx \frac{V_t}{V_t} = 1$$

Rearranging,

$$I_{D1} = I_D + \frac{\Delta I_D}{2} \quad \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right) + \frac{\Delta(W/L)}{2} \quad V_{t1} = V_t + \frac{\Delta V_t}{2}$$

$$I_{D2} = I_D - \frac{\Delta I_D}{2} \quad \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right) - \frac{\Delta(W/L)}{2} \quad V_{t2} = V_t - \frac{\Delta V_t}{2}$$

Plug these into the current equation:

$$I_{D1} = I_D + \frac{\Delta I_D}{2}$$

$$= \frac{1}{2} \mu_n C_{ox} \left[\left(\frac{W}{L}\right) + \frac{\Delta(W/L)}{2} \right] \left[V_{GS} - V_t - \frac{\Delta V_t}{2} \right]^2$$

$$= \frac{1}{2} \mu_n C_{ox} \left[\left(\frac{W}{L}\right) + \frac{\Delta(W/L)}{2} \right] \left[V_{OV}^2 - 2 V_{OV} \frac{\Delta V_t}{2} + \frac{\Delta V_t^2}{4} \right]$$

$$= \frac{1}{2} \mu_n C_{ox} \left[\left(\frac{W}{L}\right) V_{OV}^2 + \frac{\Delta(W/L)}{2} V_{OV}^2 - (W/L) V_{OV} \Delta V_t - \frac{\Delta(W/L)}{2} V_{OV} \Delta V_t \right]$$

$$= \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) V_{OV}^2 + \frac{1}{2} \mu_n C_{ox} V_{OV}^2 \left[\frac{\Delta(W/L)}{2} - \frac{(W/L)}{V_{OV}} \Delta V_t \right]$$

$$\frac{\Delta I_D}{2} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) V_{OV}^2 \left[\frac{1}{2} \frac{\Delta(W/L)}{(W/L)} - \frac{\Delta V_t}{V_{OV}} \right]$$

$$\therefore \frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{(W/L)} - \frac{\Delta V_t}{(V_{OV}/2)}$$

Fractional
Current
Mismatch

Geometry (i.e., Layout)
Based Component

↑
Independent of
Bias Point!

Increases (i.e., gets
worse) as V_{OV} is
reduced!

Today: $V_{DD} \downarrow \rightarrow V_{OV} \downarrow$
→ w/ each generation of
technology → matching more
difficult!