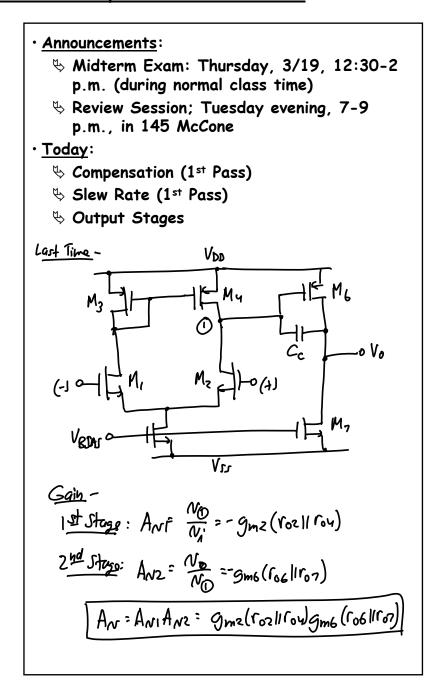
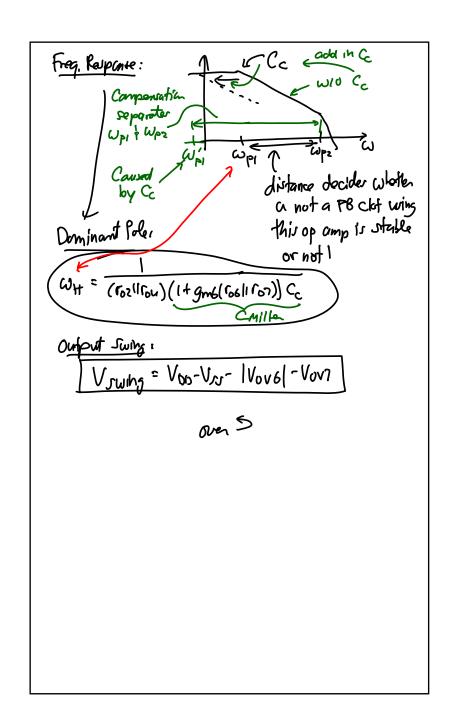
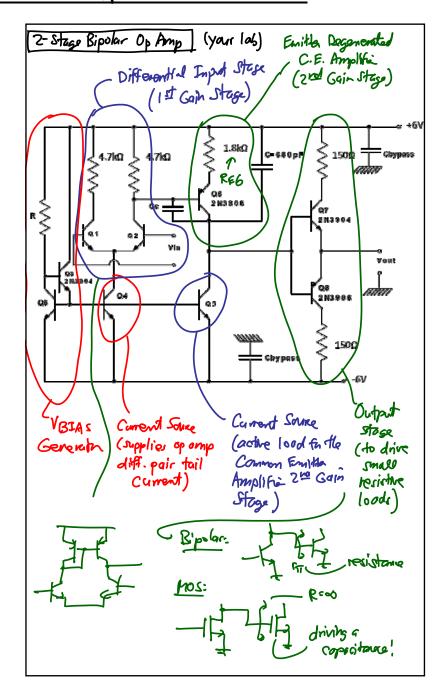
Lecture 17: Compensation & Slew Rate



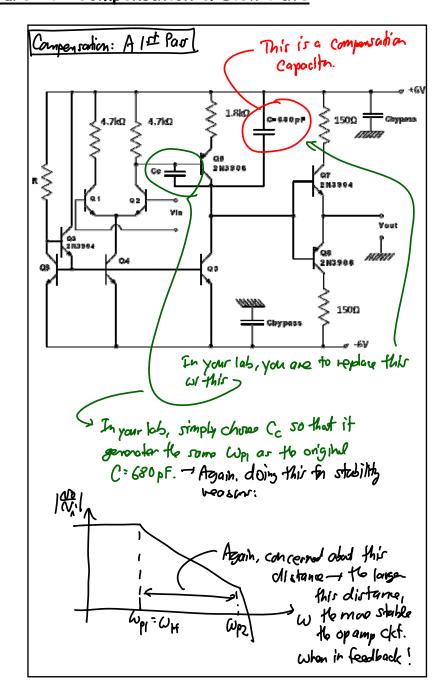


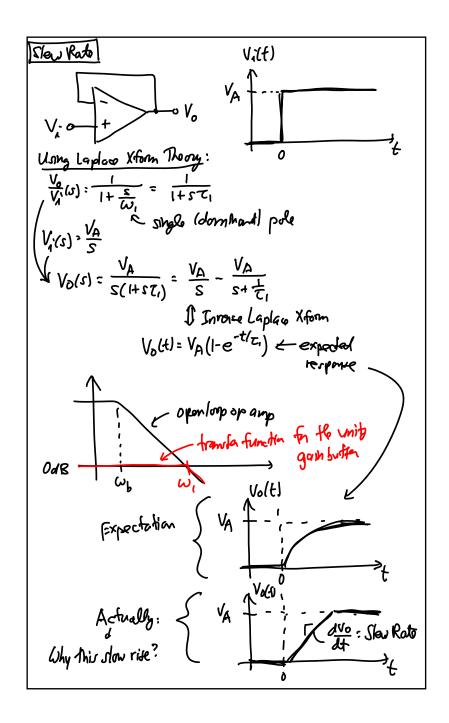
EE 140: Analog Integrated Circuits
Lecture 17: Compensation & Slew Rate



Remarks. 1) You analyze this in Lab#2. 1 Usually, the restrictly-loaded diff. poir is replaced we an octive current mirra load for more gain. 3 Reg raises the input R of Q6 (of the 2nd gain stage), plus help wil biosing. 9 Same comment as 3 for the output stage. 3 Output stage needed whom driving a restative load often to case for bipoler not often the case for Mos, whose a Capacitive load CL is often more relevant - Mos op a myer often duit need output stages! over 5

EE 140: Analog Integrated Circuits
Lecture 17: Compensation & Slew Rate





EE 140: Analog Integrated Circuits
Lecture 17: Compensation & Slew Rate

