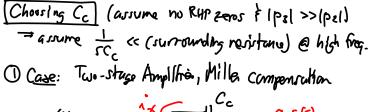
<u>EE 140: Analog Integrated Circuits</u> <u>Lecture 22: CMOS Op Amp Compensation</u>

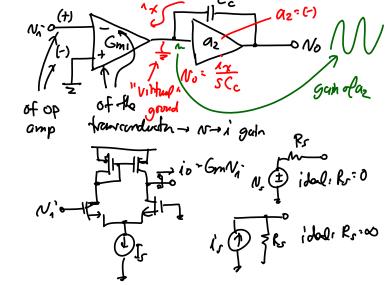
• <u>Announcements</u>:

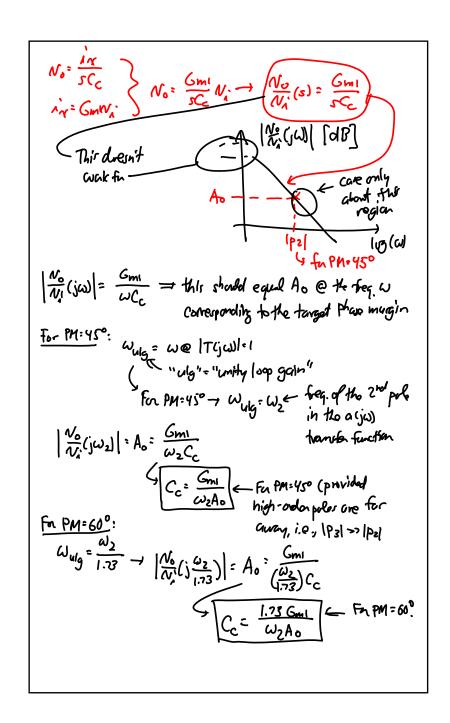
- Sour project cannot use ideal current sources; all you have is Vdd and Vss
- ✤ You need to design your own current sources if you need them
- You should also try to minimize area, as usual (e.g., a design using an enormous resistor will not be as good as one using a much smaller one, or no resistor at all)

• <u>Today</u>:

& CMOS Op Amp Compensation

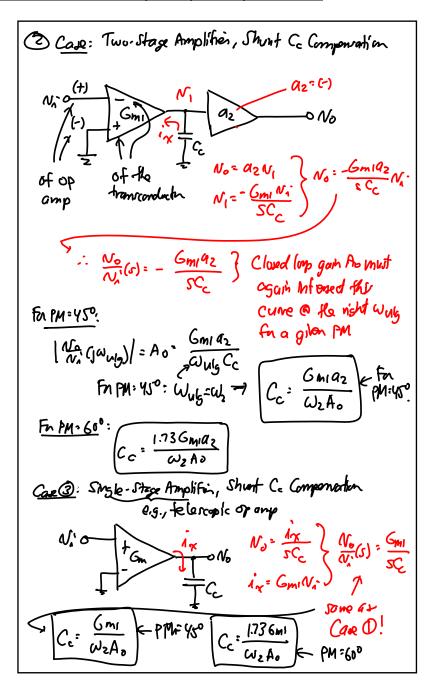


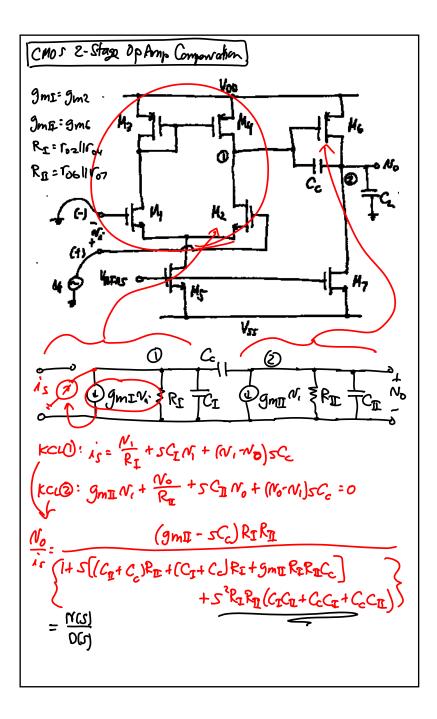




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<u>EE 140: Analog Integrated Circuits</u> Lecture 22: CMOS Op Amp Compensation

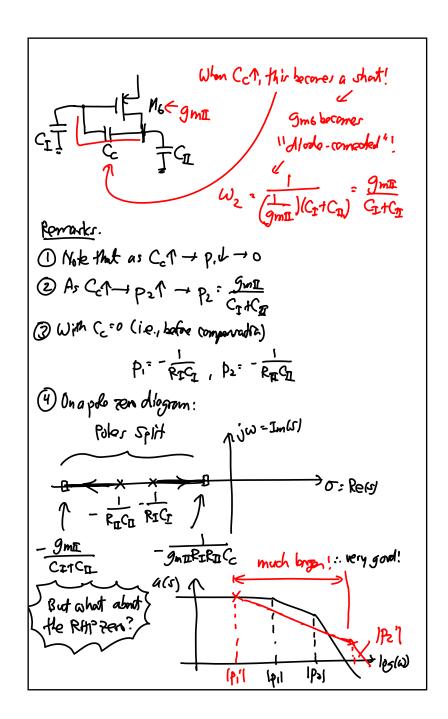




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<u>EE 140: Analog Integrated Circuits</u> <u>Lecture 22: CMOS Op Amp Compensation</u>

This Xfon fin has 2 poler & a zero! The zero: $N(s) = 0 \xrightarrow{\pi} \left| Z : \frac{g_{mII}}{C_{r}} \right| \leftarrow (+) \text{ good Real}$ The poles: $DkJ = \left(1 - \frac{S}{P_{1}}\right)\left(1 - \frac{S}{P_{2}}\right) = 1 - S\left(\frac{1}{P_{1}} + \frac{1}{P_{2}}\right) + \frac{S^{2}}{P_{1}P_{2}}$ $\left[p_{2}\ggp_{1}\right] \approx 1-\frac{5}{p_{1}}+\frac{5^{2}}{p_{1}p_{2}}$ (i.e., p. is a dominant pule S. Thus: $P_{i} = -\frac{1}{(C_{II}+C_{c})R_{II} + (C_{I}+C_{c})R_{I} + gm \overline{u}R_{I}R_{I}C_{c}}$ $As C_{c} \uparrow \rightarrow p_{i} \downarrow \rightarrow \approx -\frac{1}{gm_{L}R_{I}R_{I}C_{c}}$ For the 2nd pole: $P_{IP_{z}} = \frac{1}{R_{I}R_{I}(C_{I}C_{I}+C_{L}+C_{c}C_{I})}$ $P_2 \stackrel{\text{\tiny def}}{=} - \frac{g_{\text{MIL}}C_c}{C_{\text{E}}C_{\text{E}} + C_c} + C_c}$ G As $C_c \uparrow - P_2 \cong - \frac{g_{\text{MII}}}{C_{\text{I}} \uparrow C_{\text{II}}} \subset This is history$ than before! $C_c \uparrow \rightarrow p_z \Gamma$



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