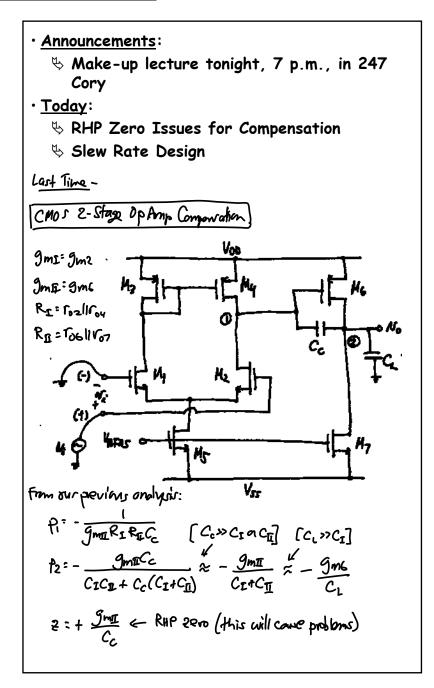
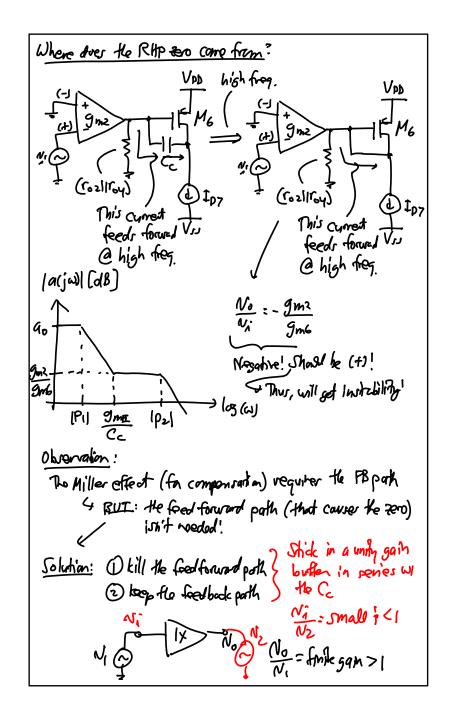
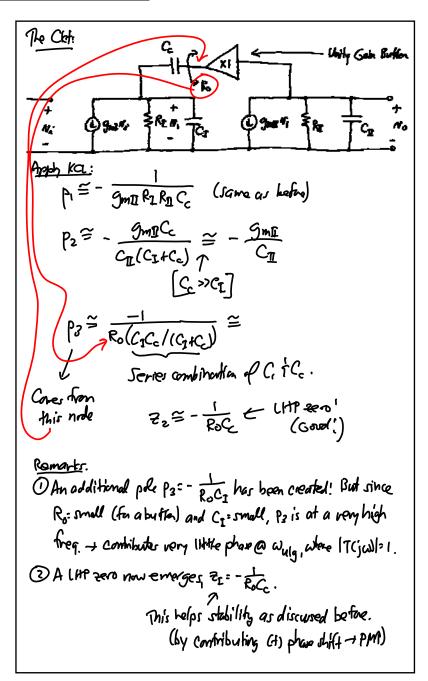
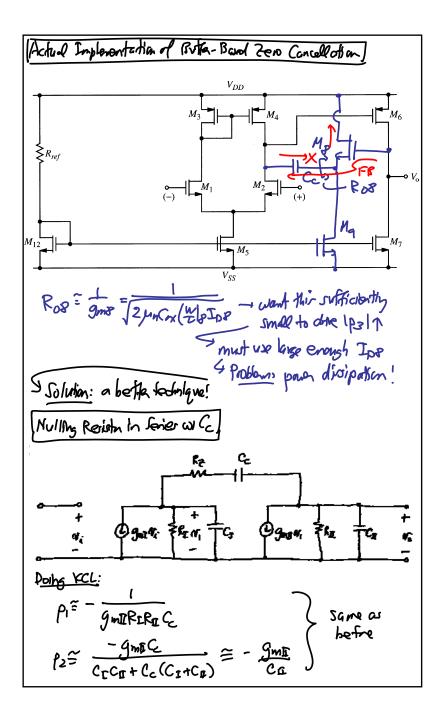
<u>EE 140: Analog Integrated Circuits</u> <u>Lecture 23: RHP Zero</u>

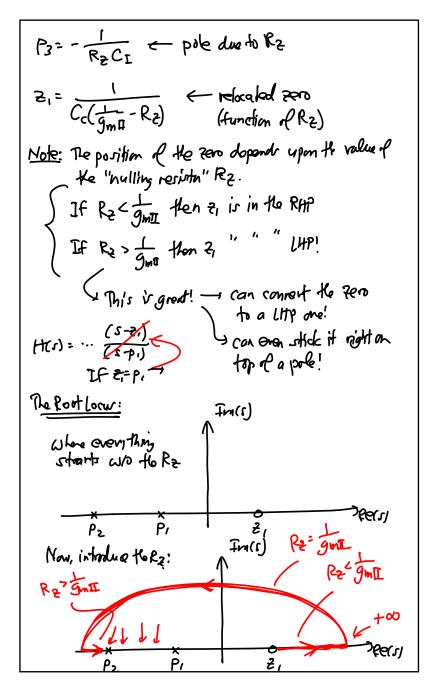






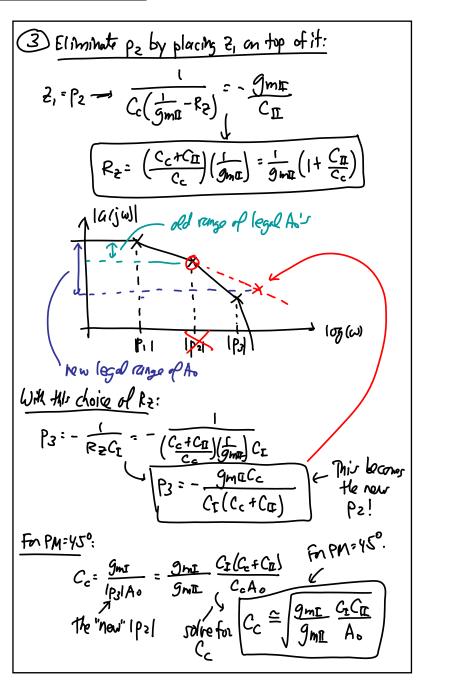


<u>EE 140: Analog Integrated Circuits</u> <u>Lecture 23: RHP Zero</u>



Zero Placement Stratesies] 1) Eliminati 2, - more it to 00: $Z_{1} = \frac{1}{C_{c}(\frac{1}{q_{ma}} - R_{z})} \rightarrow \infty \quad \text{when} \quad \begin{bmatrix} R_{z} & \frac{1}{g_{ma}} \\ & g_{ma} \end{bmatrix} \quad \text{(red} \quad g_{cq}$ $\begin{array}{c} \overbrace{After doing this: } P_3 \stackrel{\sim}{=} - \underbrace{g_{hD}}{C_{I}} \\ This is gove...} \\ F_2 \stackrel{\sim}{=} - \underbrace{g_{mE}}{C_{II}} \\ F_2 \stackrel{\sim}{=} - \underbrace{g_{mE}}{C_{$ do botton-(2) Eliminate p3 by placing Z, on top of it: $\mathcal{Z}_{1} = \beta_{3} \xrightarrow{=} C_{c} \left(\frac{1}{g_{MT}} - R_{z} \right)^{z} - \frac{1}{R_{z}C_{L}}$ $R_2 = \frac{1}{g_{m_2}(1 - \frac{C_I}{2})}$ 1) p3 gone, p1 + p2 left (2) Now, can place Wulg @ p2 and really got AM= 45. (aro worrying about the influence of P3) But can still do better than this. 5 Non

<u>EE 140: Analog Integrated Circuits</u> <u>Lecture 23: RHP Zero</u>



FG PM=60 : $C_{c} = \frac{1.73}{1} \frac{g_{mE}}{f_{s} | A_{o}} \xrightarrow{T_{1}} C_{c} \cong \int \frac{1.73}{g_{mE}} \frac{C_{c}C_{c}}{g_{mE}} \frac{C_{c}C_{c}}{A_{o}} \frac{C_{c}C_{c}}{f_{mE}} \frac{C_{c}C_{c}}{f_{o}}$ Remark. If soffling time is important, then approach 3 may not be the best approach. The reason is that if the zero is not exactly. equal to the ple, the a "doublet" envires, which actually can hunt the settling time. Discupat in a hondout to be pasted on the Course adulte. - also, discussed in Razavi, problem 10.19. Actual Implementation = resistor are too bis! - : implement using a much malle Mar resista! MOS Resister: just an MOS Xrista openated in the linear region ς $I_{d} = \mu_{n} C_{x} \frac{W}{U} \left[(V_{gs} - V_{4}) V_{ds} - \frac{1}{2} V_{ds}^{2} \right]$ Id Slave Vos Ve Orde Un Crit (Vos Ve Vds) linear $R_{S,S} = \left[\frac{dId}{dV_{ds}}\right]^{-1} = \frac{1}{\mu_{0}G_{7}} \frac{W}{L} \left(V_{GS} - V_{4} - V_{DS}\right)^{2} \frac{dV}{2} \frac{dV_{0}}{dV_{0}} + \frac{1}{2} \frac{1}{V_{0}} \frac{W}{L} \left(V_{0} - V_{0}\right)^{2} \frac{1}{2} \frac{dV_{0}}{dV_{0}} + \frac{1}{2} \frac{1}{V_{0}} \frac{1}{V_{0}} \frac{W}{L} \left(V_{0} - V_{0}\right)^{2} \frac{1}{2} \frac{1}{V_{0}} \frac{1}{V_{0$ a Variable resister cartollale by Vos!