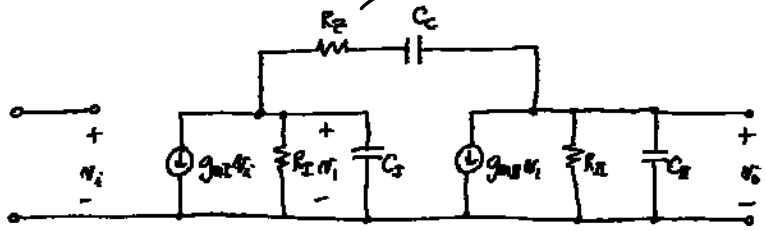
- **Today:**
  - RHP Zero Issues for Compensation (cont.)
  - Slew Rate II (design)
  - Settling Time

Last Time -

Nulling Resistor in Series w/ C_c

$$z_1 = \frac{1}{C_c\left(\frac{1}{g_{mII}} - R_z\right)}$$



Zero Placement Strategies

① Eliminate z_1 → move it to ∞.

② Eliminate p_3 by placing z_1 on top of it.

③ Eliminate p_2 by placing z_1 on top it.
↳ most attractive... but...

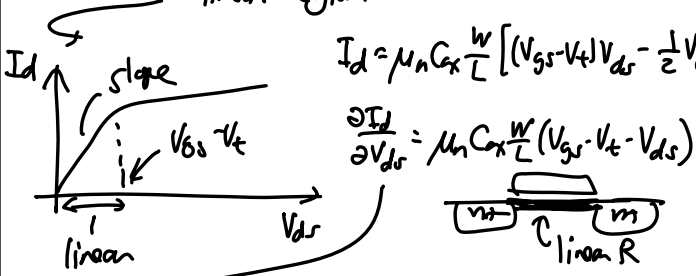
Remark: If settling time is important, then approach ③ may not be the best approach. The reason is that if the zero is not exactly equal to the pole, then a "doublet" ensues, which actually can hurt the settling time.

Discussed in a handout to be posted on the course website. → also discussed in Razavi, problem 10.19.

Actual Implementation

⇒ resistor are too big! → ∴ implement using a much smaller MOS resistor!

MOS Resistor: just an MOS Xistor operated in the linear region



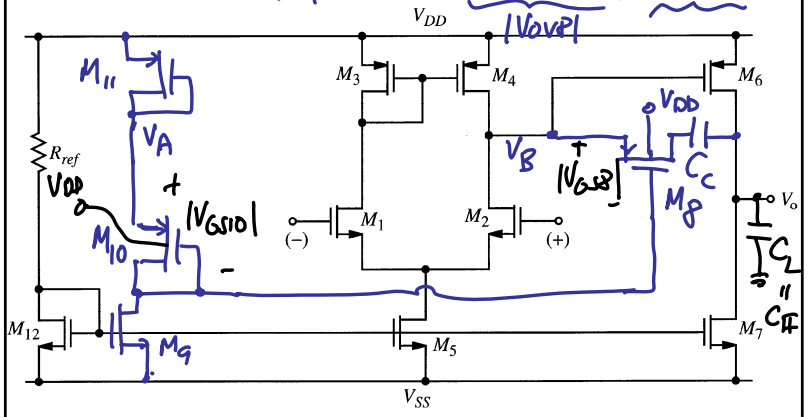
$$R_{s.s.} = \left[\frac{dI_d}{dV_{ds}}\right]^{-1}_{V_{GS}=V_{GS},\,V_{ds}=V_{DS}} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t-V_{DS})} = \frac{1}{g_{ds}}$$

a variable resistor controllable by V_{GS}!

Actual Implementation

$V_{DS8} = 0V \Rightarrow R_8 = \frac{1}{\mu_p C_{ox}(W/L)_8(|V_{GS8}| - |V_{t8}|)}$ ($|V_{GS8}| - |V_{t8}| = |V_{ov8}|$)

Replicate This



Design.

Need $V_A = V_B \rightarrow |V_{GS11}| = |V_{GS6}|$, know that $|V_{t11}| = |V_{t6}|$

$$\sqrt{\frac{2I_{D11}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{11}}} = \sqrt{\frac{2I_{D6}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_6}}$$

$$\left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_6 \frac{I_{D11}}{I_{D6}} = \left(\frac{W}{L}\right)_6 \frac{I_{D10}}{I_{D6}}$$

Also need $|V_{GS10}| = |V_{GSP}|$

Because $V_A = V_B \rightarrow V_{S10} = V_{SP} \rightarrow |V_{t10}| = |V_{tP}|$

$$\therefore |V_{OV10}| = |V_{OVP}| = \sqrt{\frac{2I_{D10}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{10}}}$$

Thus:

$$R_S = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_8 \sqrt{\frac{2I_{D10}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{10}}}} = \frac{\sqrt{\mu_p C_{ox}(W/L)_{10}}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_8 \sqrt{2I_{D10}}}$$

Case: Elimate p_2 by placing z_1 on top of it.

$$R_Z = \frac{C_c + C_L}{g_{m6} C_c} = \frac{\sqrt{\mu_p C_{ox}(W/L)_{10}}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_8 \sqrt{2I_{D10}}}$$

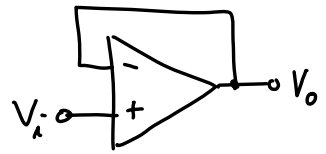
$$\sqrt{2\mu_p C_{ox}(W/L)_6 I_{D6}}$$

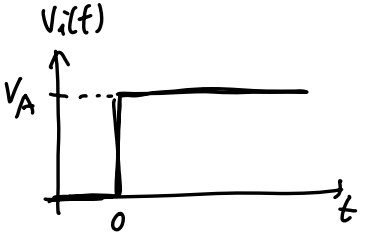
$$\left(\frac{W}{L}\right)_8 = \sqrt{\left(\frac{W}{L}\right)_6 \left(\frac{W}{L}\right)_{10} \frac{I_{D6}}{I_{D10}} \cdot \left(\frac{C_c}{C_c + C_L}\right)}$$

Case: Move $z_1 \rightarrow \infty$.

$$R_Z = \frac{1}{g_{m6}} \Rightarrow \left(\frac{W}{L}\right)_8 = \sqrt{\left(\frac{W}{L}\right)_6 \left(\frac{W}{L}\right)_{10} \frac{I_{D6}}{I_{D10}}}$$

Slew Rate (from before)





Using Laplace Xform Theory:

$$\frac{V_o}{V_i}(s) = \frac{1}{1 + \frac{s}{\omega_1}} = \frac{1}{1 + s\tau_1}$$

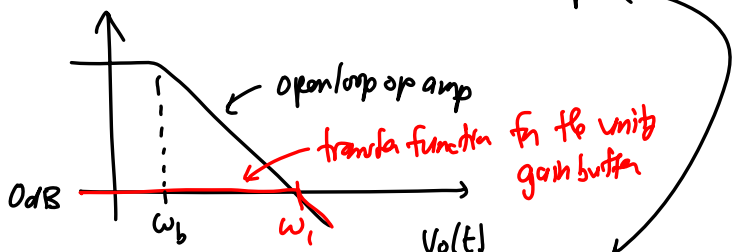
↖ single (dominant) pole

$$V_i(s) = \frac{V_A}{s}$$

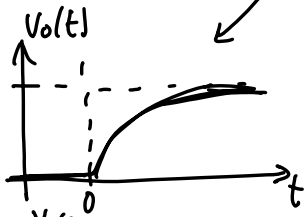
$$V_o(s) = \frac{V_A}{s(1 + s\tau_1)} = \frac{V_A}{s} - \frac{V_A}{s + \frac{1}{\tau_1}}$$

⇕ Inverse Laplace Xform

$$V_o(t) = V_A(1 - e^{-t/\tau_1})$$ ← expected response

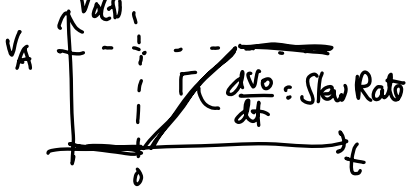


Expectation

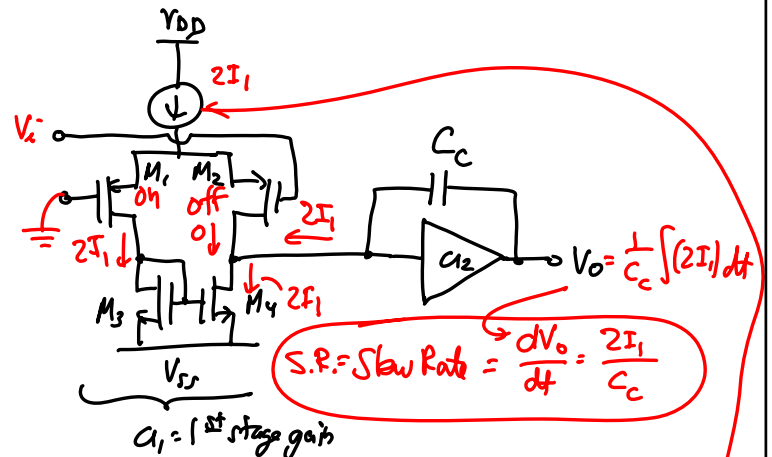


Actually:

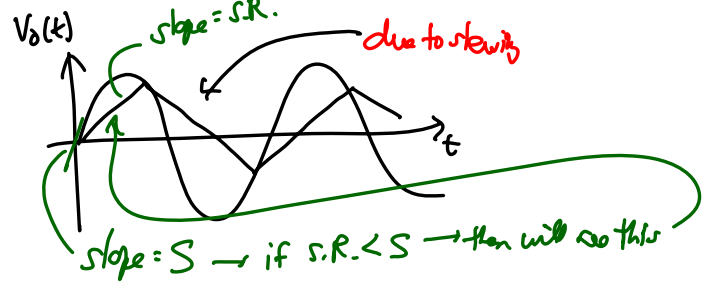
Why this slow rise?



Reason: 1st & 2nd stage of op amp cannot source enough current to mimic the slope (or speed) of a fast rising input signal.



If apply a very fast (i.e., high freq., large amplitude) sinusoid:



In terms of design variables:

$$S.R. = \frac{dV_o}{dt} = \frac{I_{xm}}{C_c} = \boxed{\frac{I_{xm}}{G_{m1}} \omega_{ulg} A_0 = S.R.}$$

C_c ↑

$$C_c = \frac{G_{m1}}{\omega_{ulg} A_0}$$ ← closed loop gain

($\omega_{ulg} = \omega$ @ $|T(j\omega)| = 1$)

To Increase S.R.:

① Decrease G_{m1} ← transconductance of 1st stage

② Increase ω_{ulg} → increase ω_2
↘ limited by the existing freq. range

③ Use a larger A_0, if possible.
↓
closed loop gain (only if permitted by the application)

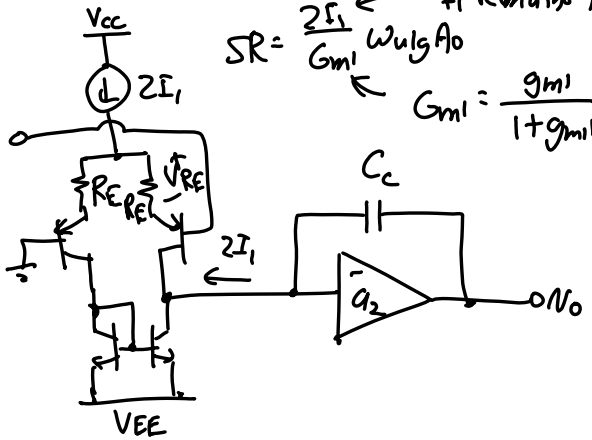
Increasing S.R. via G_m-Reduction

① Emitter or Source Degeneration of the Input Stage

I_1 remains the same

$$SR = \frac{2I_1}{G_{m1}} \omega_{ulg} A_0$$

$$G_{m1} = \frac{g_{m1}}{1 + g_{m1} R_E} \downarrow \rightarrow SR \uparrow$$



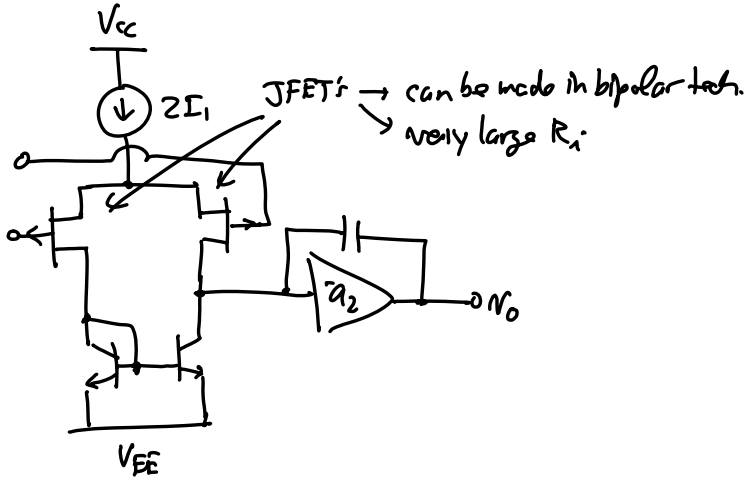
Limitations:

① R_E mismatch → V_{os}
↓ must limit V_{RE} to limit V_{os}

② R_E↑ → gain↓ (SR-gain trade-off)

③ R_E contributes thermal noise → must limit to preserve the noise performance of the op amp.

② FET Input Devices -



For FET's: $\frac{g_m}{I_D} \simeq \frac{2}{V_{GS}-V_t}$ ← ~0.2V

For BJT's: $\frac{g_m}{I_C} = \frac{1}{V_T}$ ← 26mV

$$\frac{\text{FET S.R.}}{\text{BJT S.R.}} = \frac{\frac{I_D}{g_{mF} W_1 C_1}}{\frac{I_C}{g_{mB} W_1 C_1}} = \frac{\frac{V_{GS}-V_t}{2}}{V_T} = \frac{V_{GS}-V_t}{2V_T} = \frac{260}{26} \approx 10$$

Limitations:

① Higher V_{OS}.

② Increased voltage noise.
(But decreased current noise.)

Settling Time

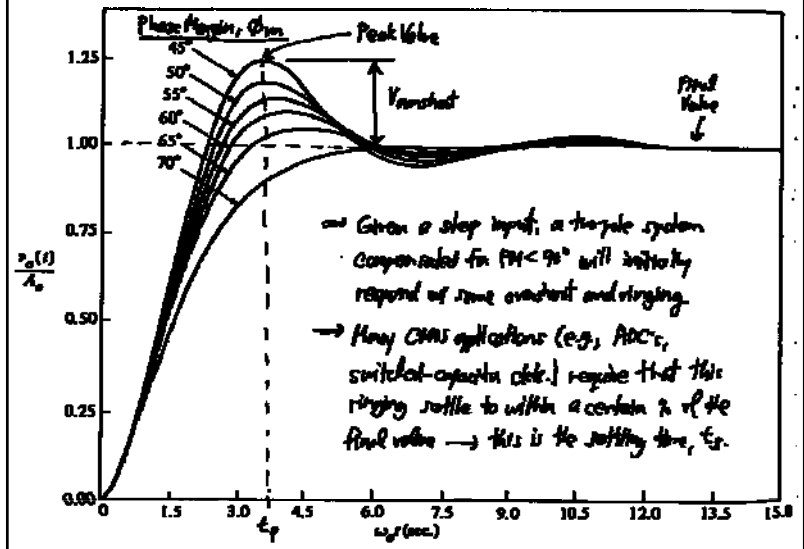
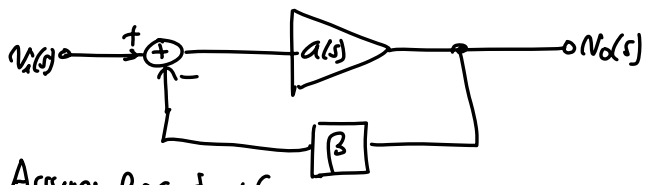


Figure 8.2-3 Response of second-order system with various phase margins.

Obtain Expressions for:

① $V_{overshoot}$
② Settling Time, T_s
} as functions of phase margin, ϕ_m



Assume: β = const w/ freq.

$$A(s) = \frac{V_o(s)}{V_i(s)} = \frac{a(s)}{1 + a(s)\beta}$$

$$a(s) = \frac{a_0}{\left(1+\frac{s}{\omega_1}\right)\left(1+\frac{s}{\omega_2}\right)} = \frac{a_0 \omega_1 \omega_2}{(s+\omega_1)(s+\omega_2)}$$

$$A(s) = \frac{a_0 \omega_1 \omega_2}{s^2 + (\omega_1 + \omega_2)s + \omega_1 \omega_2 (1 + a_0 \beta)}$$

$$= \frac{A_0 \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{A_0 \omega_0^2}{s^2 + \left(\frac{\omega_0}{Q}\right)s + \omega_0^2}$$

$$[\omega_0 = \omega_n]$$

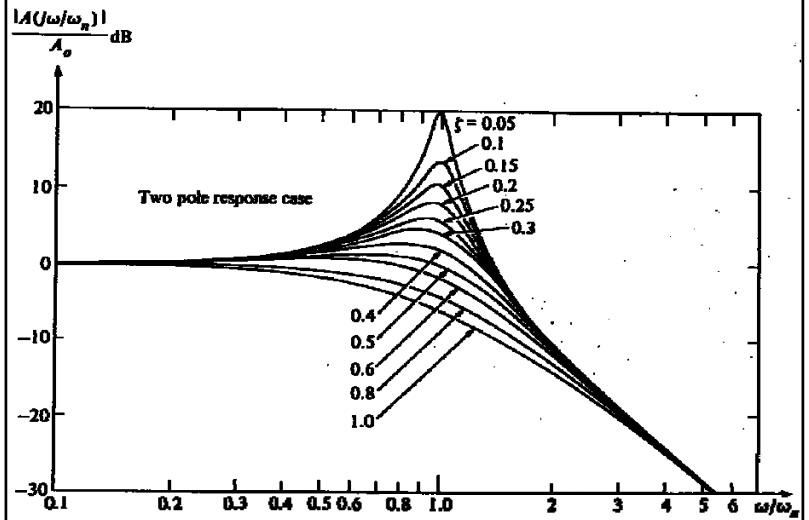
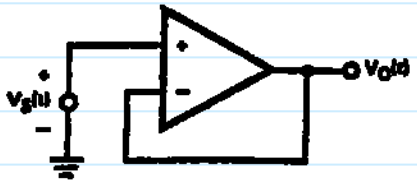


Figure C-2 Gain magnitude response for various values of ζ for a second-order, low-pass system.

Asymmetrical Slew Rate

Very often the SR is not symmetrical in some FB ckts.

→ SR can be different for (+)ve & (-)ve going output signals



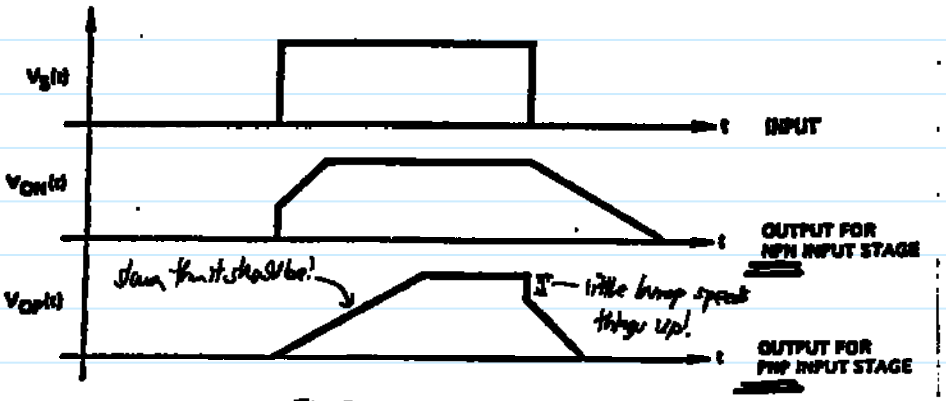


Fig. 8.1

Fig. 16. Large signal response of the voltage follower. For an op amp with simple n-p-n input stage we get the waveform $v_{on}(t)$, which exhibits a step slew "enhancement" on the positive going output, and a slew "degradation" on the negative going output. For a p-n-p input stage, these effects are reversed as shown by $v_{op}(t)$.

Analyze the slewing conditions for the pnp input stage:

Slew "Degradation"

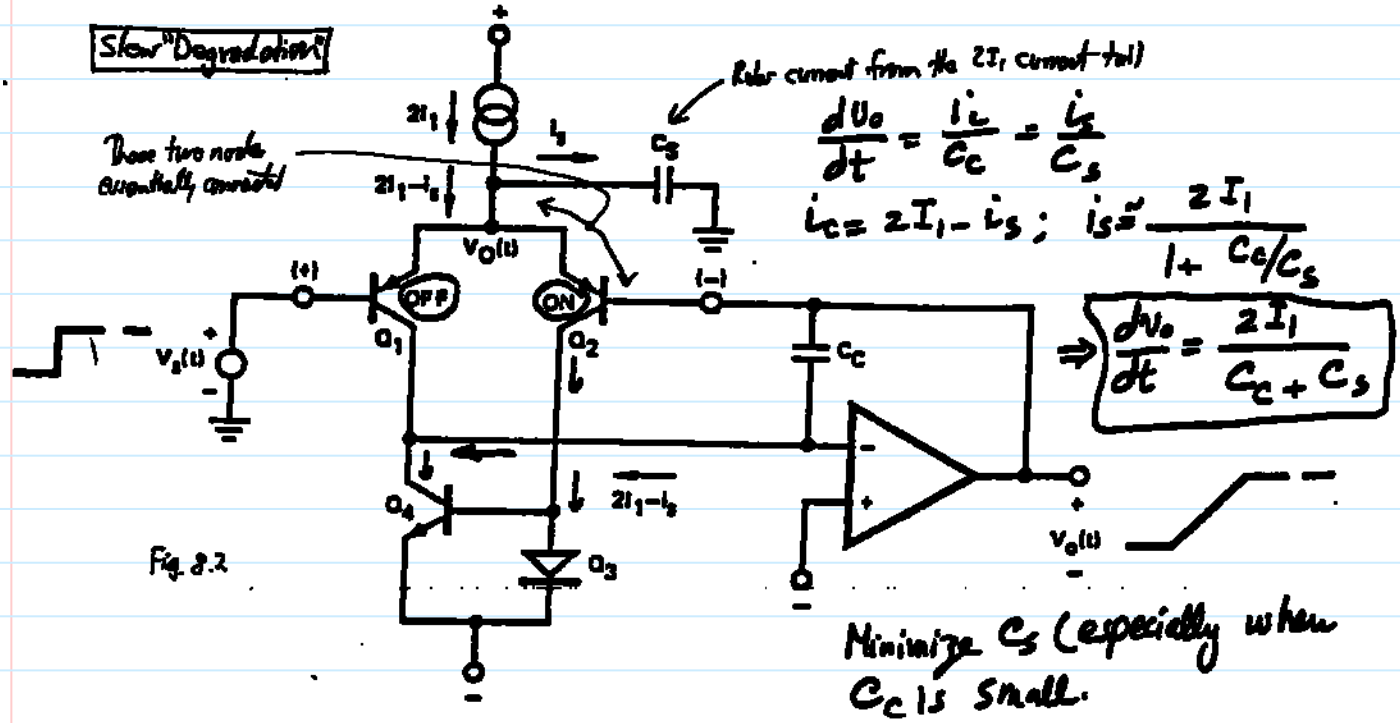


Fig. 8.2

$$\frac{dV_o}{dt} = \frac{i_c}{C_c} = \frac{i_s}{C_s}$$

$$i_c = 2I_1 - i_s \; ; \; i_s = \frac{2I_1}{1 + C_c/C_s}$$

$$\Rightarrow \frac{dV_o}{dt} = \frac{2I_1}{C_c + C_s}$$

Minimize C_s (especially when C_c is small.

Slew "Enhancement"

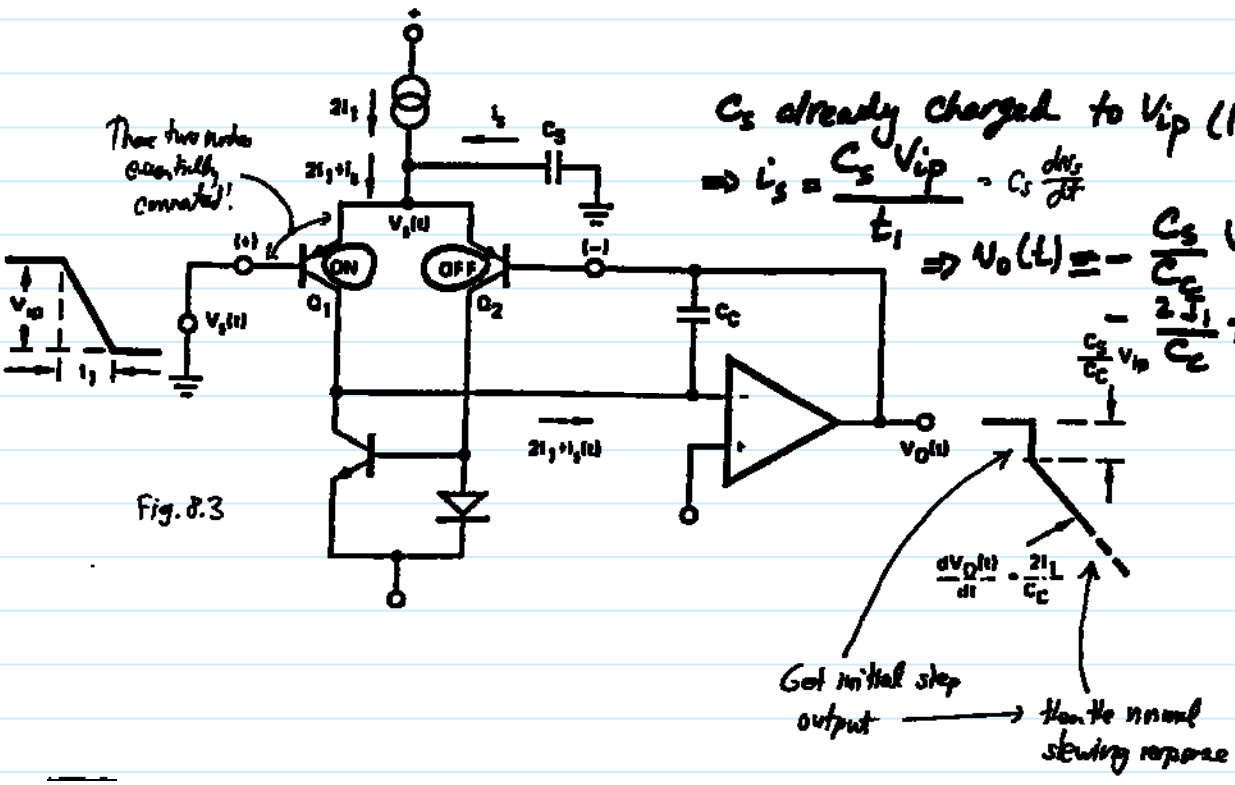


Fig. 8.3