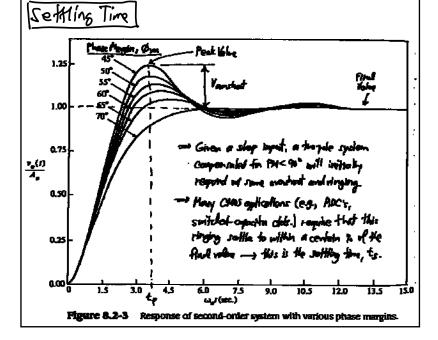
## Announcements:

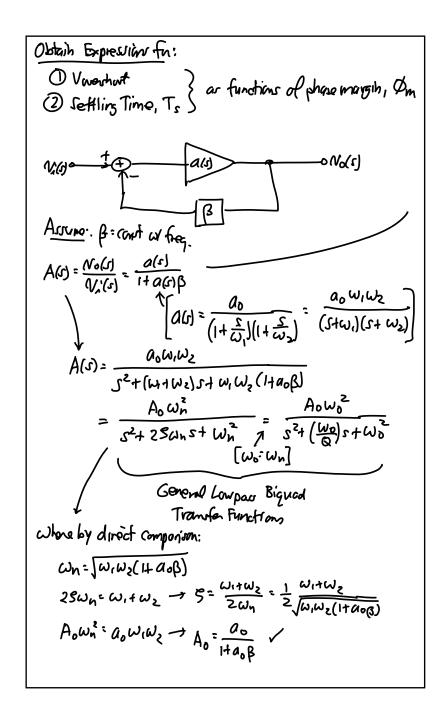
- As has been announced previously, there will be no lecture next week (this is why we've been having evening lectures)
- \$\text{There will still be discussion and labs}
- Mehmet will take Yang's discussion and lab sections, since Yang will also be gone
- ♥ HW#10 is due the week after next
- Use the smaller HW load to finish your project

## · Today:

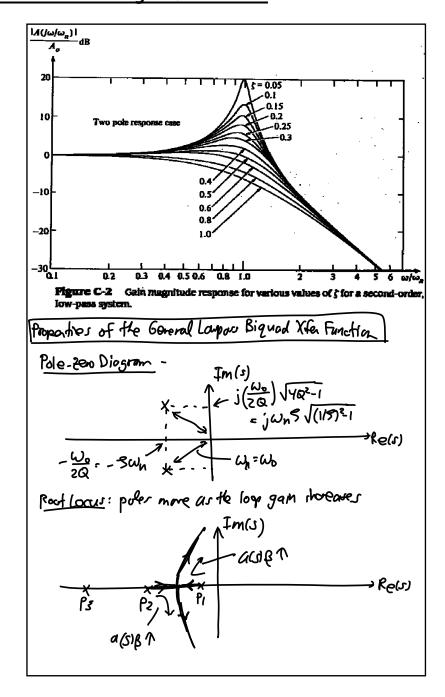
- ♦ Settling Time
- ♦ Power Supply Rejection Ratio (PSRR)

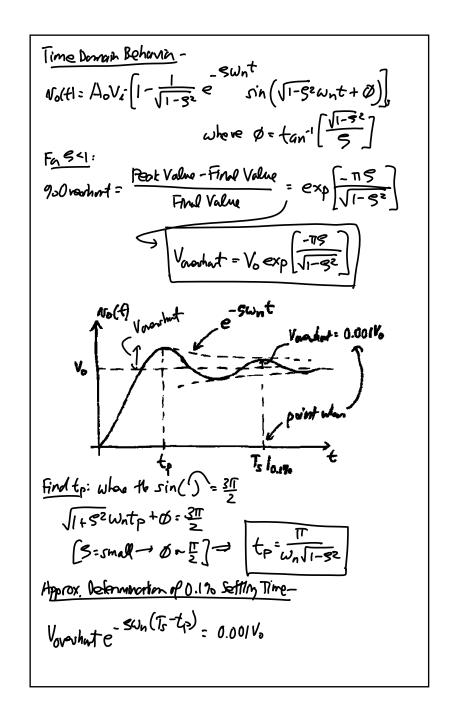
Last Time -



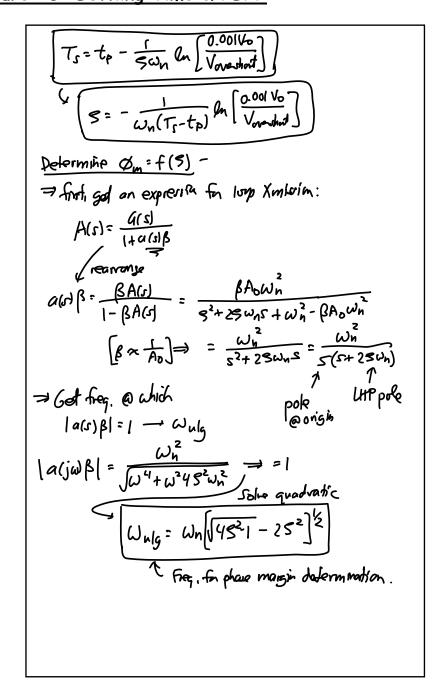


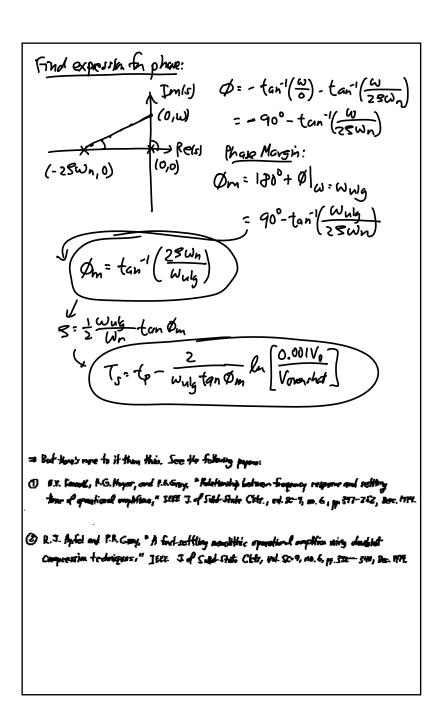
EE 140: Analog Integrated Circuits Lecture 25: Settling Time & PSRR



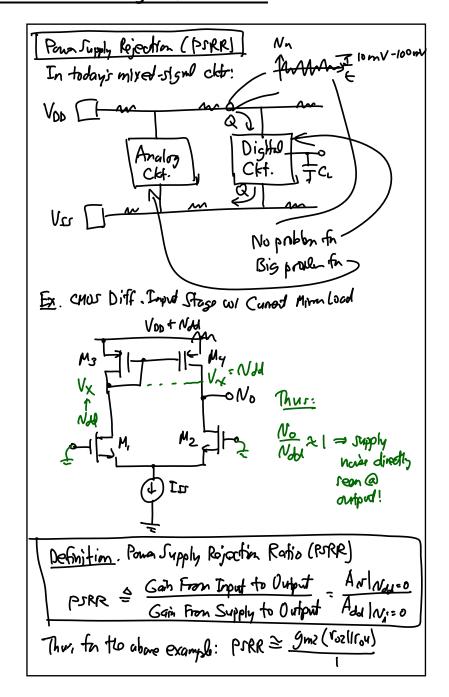


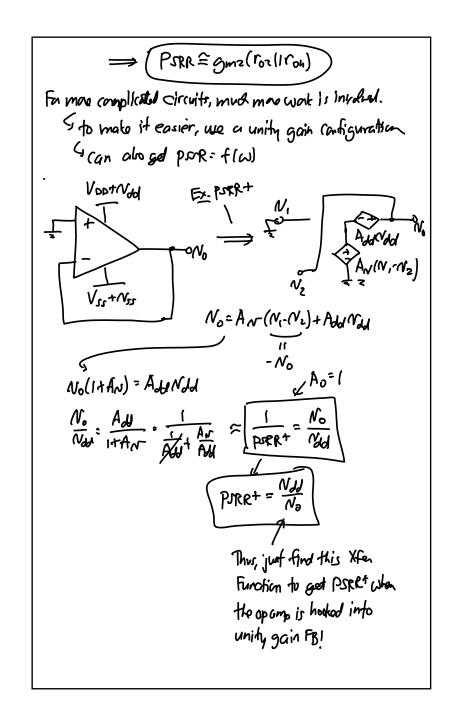
## EE 140: Analog Integrated Circuits Lecture 25: Settling Time & PSRR



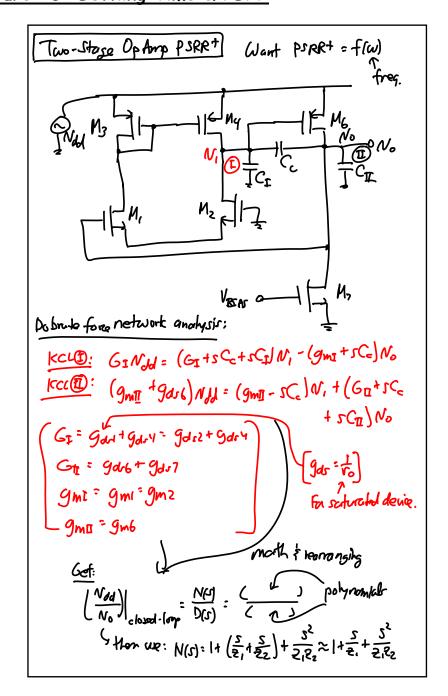


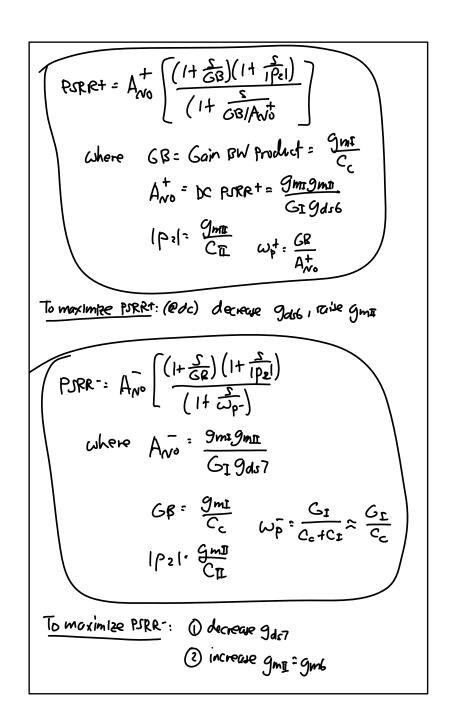
EE 140: Analog Integrated Circuits Lecture 25: Settling Time & PSRR





EE 140: Analog Integrated Circuits Lecture 25: Settling Time & PSRR





## Remarks.

① Since often gran < gurb → often PSSR->PSRR+ (edc)

$$\frac{2}{\omega_p^+} = \frac{\frac{G_1/g_c}{g_{abc}}}{\frac{G_1 g_{abc}}{g_{mu} G_c}} = \frac{g_{mu}}{g_{abc}} \rightarrow \text{thetis quite large}$$

$$\therefore \omega_p^- \gg \omega_p^+$$

Thus, for an NMOS input of omp, PSR- is often better than PSRR+. - in design, need to worm more about PSRR+1

- 3 Some methods for reducing PSRR:
  - (i) Use builda-based 2010-Carcellation in the compansation loop.
  - (ii) Uso caroode circuitry, or baloncal circuit topologies.
  - (ii) Supply-independent biesty.
  - (iv) Design stategies to minimize parasitic capacitive feedthrough.