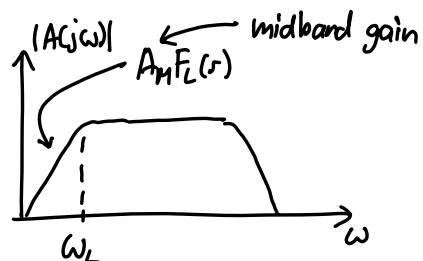


Today:

- Short-Circuit Time Constant Analysis for Low Frequency Cut-Off
- Active Loads

Last Time -



$$\omega_L \cong \omega_1 = \sum_j \omega_{pj} = \sum_j \frac{1}{C_j R_{js}} = \sum_j \frac{1}{\tau_{js}}$$

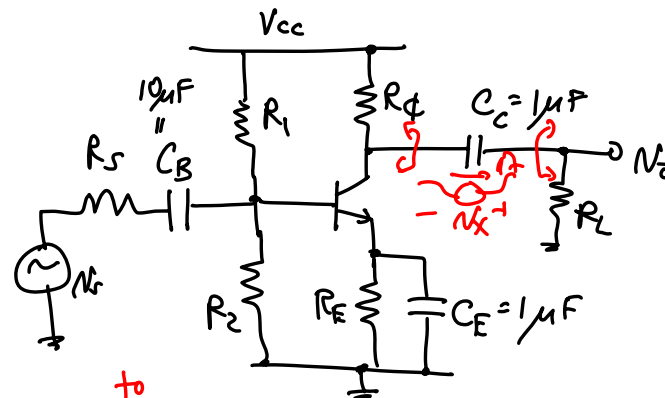
where  $C_j \triangleq$  various large ( $> 10 \text{ nF}$ ) capacitors in the ckt. (e.g., the bypass caps.)

$R_{js} \triangleq$  driving point resistance seen between

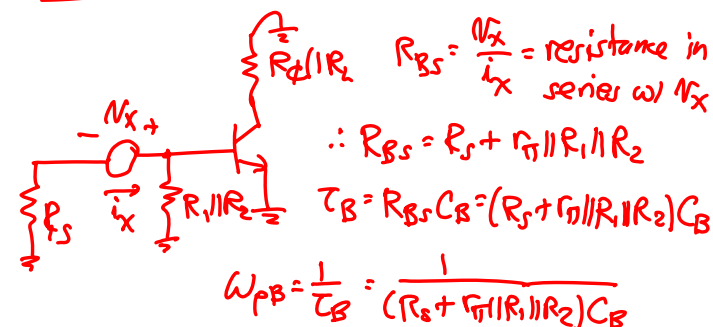
the terminals of  $C_j$  determined with:  
For readability, can go to Sedra & Smith

- ① all large capacitors short-circuited, except  $C_j$ , which is replaced by the test voltage source for  $R$  determination
- ② all independent sources eliminated (i.e., short voltage sources, open current sources)
- ③ open all H.F. capacitors (i.e., small caps in the pF range, or  $< 1 \text{ nF}$ )

Ex: Determine the L.F. Response of the C.E. Amplifier



to  
(a)  $\tau$  due to  $C_B$ : short ckt.  $C_C$  &  $C_E$



(b)  $\tau$  due to  $C_C$ : short ckt.  $C_B$  &  $C_E$   
again, it will be the  $R$  in series

$$\tau_C = (R_L + r_o \parallel R_C) C_C$$

$\sim R_C \hookrightarrow \omega_{pc} = \frac{1}{\tau_C} = \frac{1}{(R_L + R_C) C_C}$

(c)  $\tau$  due to  $C_E$ : short  $C_B$  &  $C_C$

$$R_{B||R_L} = \frac{1}{g_m} + \frac{R_S || R_1 || R_2}{\beta + 1}$$

$$R_{E||R_S} = R_E || \frac{r_{\pi} + R_B || R_L || R_E}{\beta + 1}$$

$$\tau_E = R_{E||R_S} C_E$$

$$\omega_{pE} = \frac{1}{\tau_E} = \frac{1}{R_{E||R_S} C_E}$$

and finally:

$$\omega_L = \omega_{pB} + \omega_{pC} + \omega_{pE}$$

**Active Loads**

⇒ why use  $k_{om}$ ?

For  $\frac{V_o}{V_i} \uparrow$ , must:

- 1) Raise  $g_m \rightarrow$  raise  $I_D$   
 → problem:  $V_{DD} \uparrow \rightarrow$  gate too large  
 ∴ supply  $V_{DD}$  limits to amount of gain you can get
- 2) Increase  $R_D \rightarrow$  but same problem  
 also, area  $\uparrow$

Layout:

⇒ what would be ideal?

To solve these issues, we use active load!

Diode-Connected Enhancement Load

Depletion Load

ancient  
we won't consider this

Diode-Connected PMOS Load

PMOS Current Source Load

Diode-Connected Enhancement Load

S.S. Ckt. (do by inspection)

$$R_L = \frac{1}{g_m + g_{mb}}$$

"Diode-Connected"

How about this?

S.S. Ckt.

$$i_x = -g_m v_{gs} + g_{ds}(-v_{gs}) - g_{mb} v_{bs}$$

$$= g_m (v_x - i_x R_D) + g_{mb} v_x$$

$$R_s = \frac{v_x}{i_x} = \frac{1 + g_m R_D}{g_m + g_{mb}} = \frac{1}{g_m + g_{mb}} + \frac{R_D}{1 + \eta}$$

$$R_s \approx \frac{1}{g_m} + R_D$$

...and from the top:

S.S. Ckt.

do the analysis

$$R_d = \frac{v_x}{i_x} = \frac{1}{g_m} + (1 + \eta) R_s \approx \frac{1}{g_m} + R_s$$

Thus:

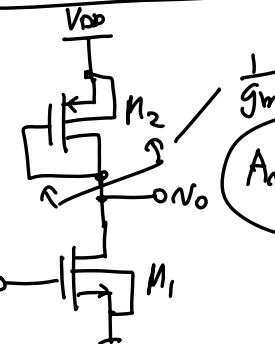
Apply to a C.S. Ckt:

$$A_v = \frac{v_o}{v_i} = \frac{-g_{m1}}{g_{m2} + g_{mb2}}$$

$$= -\frac{1}{(1 + \eta)} \frac{g_{m1}}{g_{m2}} = A_v$$

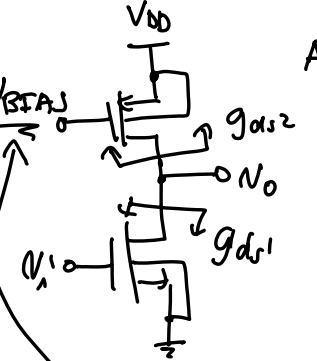
$$A_v = -\frac{1}{1 + \eta} \frac{\sqrt{2\mu_n C_{ox} (\frac{W}{L})_1 I_D}}{\sqrt{2\mu_n C_{ox} (\frac{W}{L})_2 I_D}} = -\frac{1}{1 + \eta} \sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

**Diode-Connected PMOS Load**



$$A_N = -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{\mu_n(W/L)_1}{\mu_p(W/L)_2}}$$

**PMOS Current Source Load**



$$A_N = \frac{V_o}{V_i} = -\frac{g_{m1}}{g_{ds1} + g_{ds2}} = A_N$$

$= -g_{m1}(r_{o1} || r_{o2})$

$\Rightarrow$  gain is huge! ( $r_o = \text{huge}$ )  
 $\Rightarrow$  but requires  $V_{BIAS}$