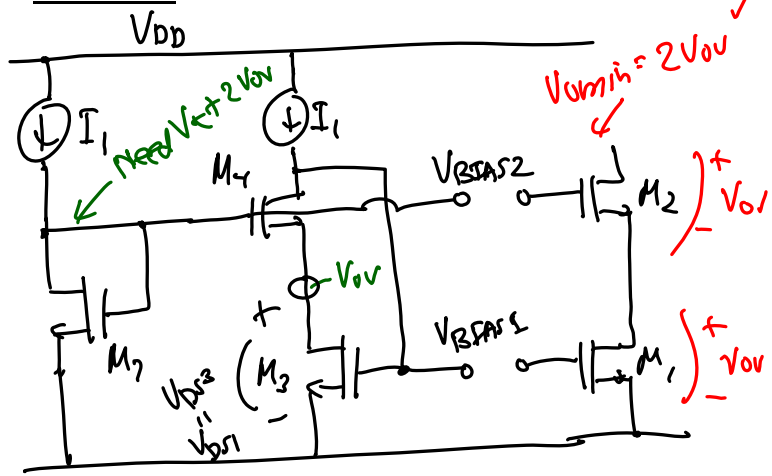
Lecture 12: DC Biasing & Current Source Matching

- **Announcements:**
  - None
- **Lecture Topics:**
  - Aside: Getting the DC Operating Point → This stuff near the end.
  - Current Source Matching Considerations
  - Op Amp Review
  - Emitter Coupled Pair (ECP)
- ----------
- **Last Time:**



$I_{D7} = I_{D3}$

$\frac{1}{2}\cancel{\mu_n C_{ox}}\left(\frac{W}{L}\right)_7 (\cancel{2V_{ov3}})^2 = \frac{1}{2}\cancel{\mu_n C_{ox}}\left(\frac{W}{L}\right)_3 (\cancel{V_{ov3}})^2$ (4)

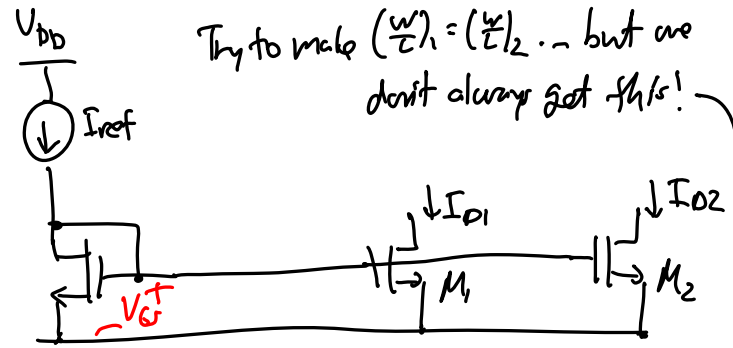
$\therefore \left(\frac{W}{L}\right)_7 = \frac{1}{4}\left(\frac{W}{L}\right)_3 = \frac{1}{4}\left(\frac{W}{L}\right)$

all the Xsistors, except M7

Note: Still must worry about Body effect!
→ must design defensively ...

$V_{GS7} > V_t + 2V_{ov3}$

Current Source Matching Considerations



Try to make $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$ ... but we don't always get this!

In MOS, we often need matched current sources: $I_{D1} = I_{D2}$

$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{t1})^2$

$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{t2})^2$

Finite fabrication tolerances in an IC process.

These aren't be perfectly matched if $(W/L)_1 \neq (W/L)_2$ & $V_{t1} \neq V_{t2}$

To quantify this:
Define average & mismatch quantities:

Average	Mismatch
$I_D = \frac{1}{2}[I_{D1} + I_{D2}]$	$\Delta I_D = I_{D1} - I_{D2}$
$\frac{W}{L} = \frac{1}{2}\left[\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2\right]$	$\Delta\left(\frac{W}{L}\right) = \left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2$
$V_t = \frac{1}{2}[V_{t1} + V_{t2}]$	$\Delta V_t = V_{t1} - V_{t2}$

$\frac{\Delta I_D}{I_D} \triangleq$ fractional current mismatch

$\frac{\Delta(W/L)}{(W/L)} \triangleq$ fractional (W/L) mismatch

$\frac{\Delta V_t}{V_t} \triangleq$ " V_t "

Rearranging:

$$I_{D1} = I_D + \frac{\Delta I_D}{2} \qquad \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right) + \frac{\Delta(W/L)}{2}$$

$$I_{D2} = I_D - \frac{\Delta I_D}{2} \qquad \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right) - \frac{\Delta(W/L)}{2}$$

$$V_{t1} = V_t + \frac{\Delta V_t}{2}$$

$$V_{t2} = V_t - \frac{\Delta V_t}{2}$$

Plug these into the current equation:

$$I_{D1} = I_D + \frac{\Delta I_D}{2}$$

$$= \frac{1}{2}\mu_n C_{ox}\left[(W/L) + \frac{\Delta(W/L)}{2}\right]\left[\overbrace{V_{GS} - V_t}^{V_{ov}} - \frac{\Delta V_t}{2}\right]^2$$

neglect small term

$$= \frac{1}{2}\mu_n C_{ox}\left[(W/L) + \frac{\Delta(W/L)}{2}\right]\left[V_{ov}^2 - 2V_{ov}\frac{\Delta V_t}{2} + \frac{\Delta V_t^2}{4}\right]$$

$$= \frac{1}{2}\mu_n C_{ox}\left[(W/L)V_{ov}^2 + \frac{\Delta(W/L)}{2}V_{ov}^2 - (W/L)V_{ov}\Delta V_t - \frac{\Delta(W/L)}{2}V_{ov}\Delta V_t\right]$$

$$= \underbrace{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{ov}^2}_{I_D} + \frac{1}{2}\mu_n C_{ox}V_{ov}^2\left[\frac{\Delta(W/L)}{2} - \frac{(W/L)}{V_{ov}}\Delta V_t\right]$$

factor out $\left(\frac{W}{L}\right)$

$$\frac{\Delta I_D}{2} = \underbrace{\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{ov}^2}_{I_D}\left[\frac{1}{2}\frac{\Delta(W/L)}{(W/L)} - \frac{\Delta V_t}{V_{ov}}\right]$$

$$\therefore \boxed{\frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{(W/L)} - \frac{\Delta V_t}{(V_{ov}/2)}}$$

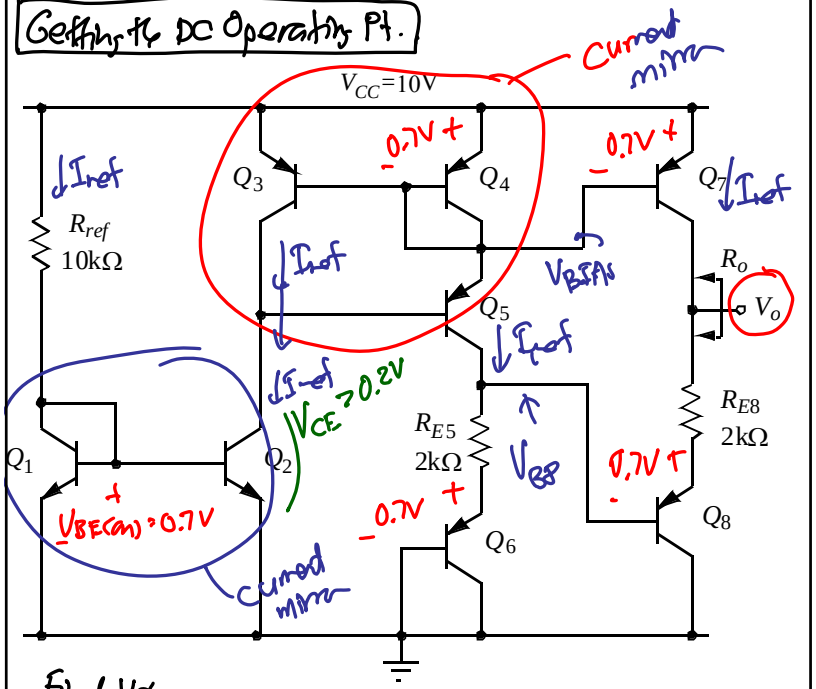
this could be (-) so this term doesn't necessarily help!

Increases (i.e., gets worse) as V_{ov} reduced!
↳ Today: $V_{ov} \to V_{ovt}$

Fractional Current Mismatch

Geometry (i.e., Layout) Based Component
↳ Indep. of bias pt.

Getting the DC Operating Pt.



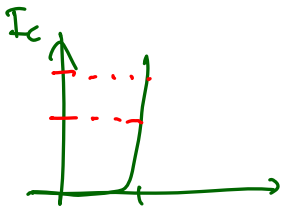
Find V_o. ← DC output voltage

Key: Find a R w/ a well-defined voltage across it.

Well-defined voltages: V_{CC}=10V, gnd, $V_{BE(on)}$

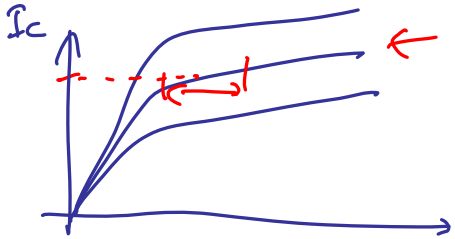
What is $V_{BE(on)}$: 0.6V or 0.7V? → Who cares!

Cannot assume $V_{BE(on)}$ = 0.7V if not forward-active. } for a forward active transistor



$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$

$V_{BE(on)}$ = 0.7 V ← well-defined



← not well defined

$$I_{ref} = \frac{V_{CC} - V_{BE(on)}}{R_{ref}}$$

$$V_{B8} = V_{BE(on)} + I_{ref} R_{E5}$$

$$V_o = V_{B8} + V_{BE(on)} + I_{ref} R_{E8}$$

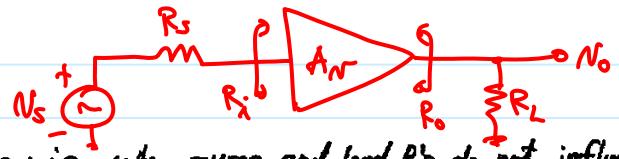
$$V_o = 2V_{BE(on)} + I_{ref}(R_{E5} + R_{E8})$$

- Start Op Amps
  - Ideal op amps
  - Diff pairs
  - Offset Voltage, Vos
  - Finite Gain
  - 2 stage op amps
  - Finite BW
  - Stability
  - Compensation of Op Amps
  - Slew Rate
  - Power Supply Rejection
  - Settling time
  - Single-stage cascade op amps for better bandwidth performance
- Some of the above is review
  - We will do the review material using pre-made lecture notes
  - Slow down for things are new to you

EE 140 — Ideal Op Amps

$$\frac{v_o}{v_s} = \underbrace{\frac{R_i}{R_i+R_s}}_{=1 \text{ when } R_i=\infty} \cdot A_v \cdot \underbrace{\frac{R_L}{R_L+R_o}}_{=1 \text{ when } R_o=0}$$

CTN



Ideal Voltage Amplifier

→ ideal when $\frac{v_o}{v_s} = A_v$; i.e., when source and load R's do not influence the gain of the amplifier.

For this to occur, the voltage division at the input & output must be eliminated. This happens when:

$R_i = \infty$, $R_o = 0$ } These resistance values define an <u>ideal voltage amplifier</u>.

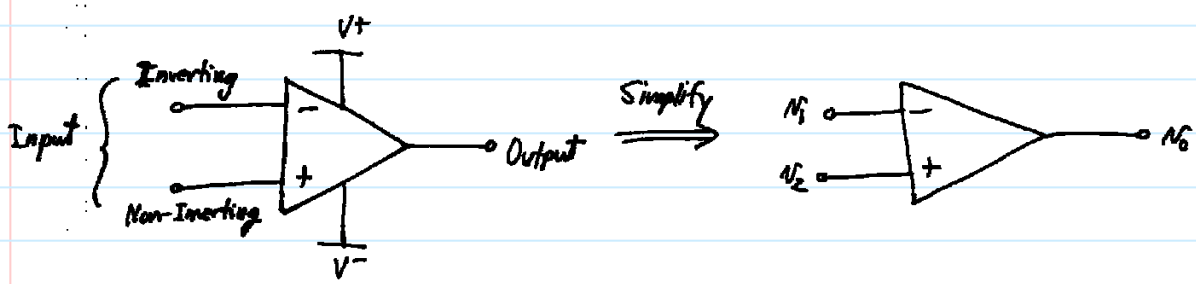
We'll look at other amplifier types later.

This, then, naturally leads us to:

Ideal Operational Amplifiers — (Op Amps)

↳ The work horse of analog electronics → combinations of op amps w/ feedback components allow the implementation of analog computers, sampled-data systems, analog filters, A/D Converters, DAC's, instrumentation amplifiers

In general, have a minimum of 5 terminals:



Perhaps the best way to define an op amp is thru its equivalent ckt:

<u>Equivalent Ckt. of an Ideal Op Amp:</u>