Lecture 25: Feedback Configurations

- Announcements:
- Design Project Checkpoint:
  - Due Monday, April 25, 11:59 p.m.
  - Send to your TA a spice file for your op amp design that simulates correctly, i.e., that reaches a stable bias point where all transistors are saturated (or linear if an MOS resistor)
  - It doesn't need to meet the project specs, but it should simulate correctly
- Lecture Topics:
  - Power Supply Rejection Ratio (PSRR) – finish w/ an example
  - Advantages of Feedback (revisited)
  - Feedback Configurations
  - Effect of FB on Z_i and Z_o
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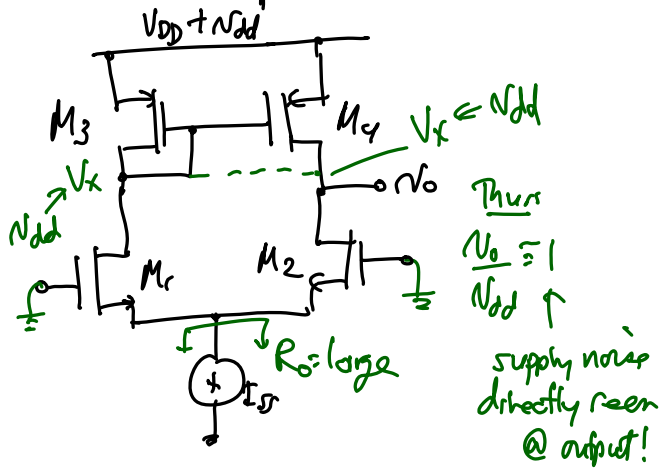
- Last Time: PSRR

Ex. CMOS Diff. Input Stage w/ Current Source Load



Thus $\frac{v_o}{v_{dd}} \cong 1$

supply noise directly seen @ output!

Definition: Power Supply Rejection Ratio (PSRR)

$$PSRR \triangleq \frac{\text{Gain from Input to Output}}{\text{Gain from Supply to Output}} = \frac{A_v|_{v_{dd}=0}}{A_{dd}|_{v_i=0}}$$

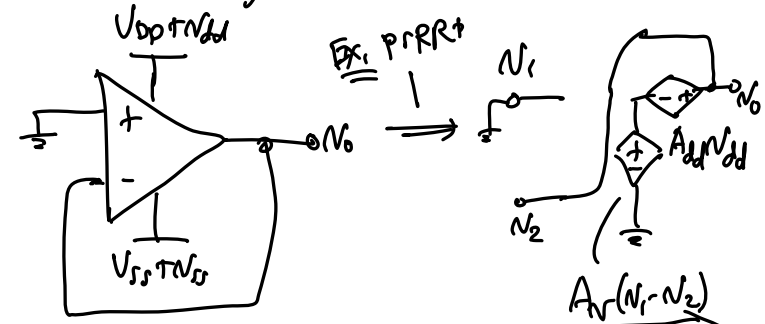
Thus, for the above example: $PSRR \cong \frac{g_{m2}(r_{o2}\|r_{o4})}{1}$

$$PSRR \cong g_{m2}(r_{o2}\|r_{o4})$$

For more complicated ckts, much more is involved.

↳ to make it easier, use a unity gain config.

↳ can also get $PSRR = f(\omega)$



$$v_o = A_v\underbrace{(v_1-v_2)}_{=-v_o} + A_{dd}v_{dd}$$

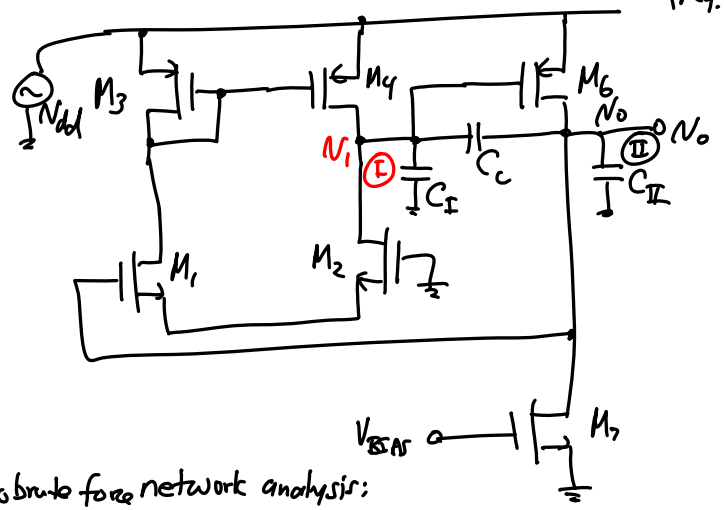
$$v_o(1+A_v) = A_{dd}v_{dd}$$

$$\frac{v_o}{v_{dd}} = \frac{A_{dd}}{1+A_v} = \frac{1}{\frac{1}{A_{dd}}+\frac{A_v}{A_{dd}}} \approx \frac{1}{PSRR^+} = \frac{v_o}{v_{dd}}$$

$$PSRR^+ = \frac{v_{dd}}{v_o}$$

Two-Stage OpAmp PSRR+

Want PSRR+ = f(ω) ← freq.



Do brute force network analysis:

KCL(I): $G_I v_{dd} = (G_I + sC_c + sC_I)v_1 - (g_{mI} + sC_c)v_o$

KCL(II): $(g_{mII} + g_{ds6})v_{dd} = (g_{mII} - sC_c)v_1 + (G_{II} + sC_c + sC_{II})v_o$

$G_I = g_{ds1} + g_{ds4} = g_{ds2} + g_{ds4}$

$G_{II} = g_{ds6} + g_{ds7}$

$g_{mI} = g_{m1} = g_{m2}$

$g_{mII} = g_{m6}$

$\left[g_{ds} = \frac{1}{r_o}\right]$ ← for saturated device.

math & rearranging

Get:

$$\left(\frac{v_{dd}}{v_o}\right)\Big|_{closed\text{-}loop} = \frac{N(s)}{D(s)} = \frac{(\quad)}{(\quad)}$$ polynomials

then use: $N(s) = 1 + \left(\frac{s}{z_1} + \frac{s}{z_2}\right) + \frac{s^2}{z_1 z_2} \approx 1 + \frac{s}{z_1} + \frac{s^2}{z_1 z_2}$

$$PSRR^+ = A_{vo}^+ \left[\frac{\left(1+\frac{s}{GB}\right)\left(1+\frac{s}{|p_2|}\right)}{\left(1+\frac{s}{GB/A_{vo}^+}\right)}\right]$$

where GB = Gain BW Product $= \frac{g_{mI}}{C_c}$

A_{vo}^+ = DC PSRR+ $= \frac{g_{mI} g_{mII}}{G_I g_{ds6}}$

$|p_2| = \frac{g_{mII}}{C_{II}}$ $\quad \omega_p^+ = \frac{GB}{A_{vo}^+}$

To maximize PSRR+: (@dc) decrease g_{ds6}, raise g_{mII}

$$PSRR^- = A_{vo}^- \left[\frac{\left(1+\frac{s}{GB}\right)\left(1+\frac{s}{|p_2|}\right)}{\left(1+\frac{s}{\omega_p^-}\right)}\right]$$

where $A_{vo}^- = \frac{g_{mI} g_{mII}}{G_I g_{ds7}}$

$GB = \frac{g_{mI}}{C_c}$ $\quad \omega_p^- = \frac{G_I}{C_c + C_I} \approx \frac{G_I}{C_c}$

$|p_2| = \frac{g_{mII}}{C_{II}}$

To maximize PSRR−: ① decrease g_{ds7}

② increase $g_{mII} = g_{m6}$

Remarks.

① Since often $g_{ds7} < g_{ds6}$ → often PSRR⁻ > PSRR⁺ (@dc)

② $$\frac{\omega_p^-}{\omega_p^+} = \frac{\cancel{C_1}/\cancel{C_c}}{\frac{\cancel{C_1} g_{ds6}}{g_{mII}\cancel{C_c}}} = \frac{g_{mII}}{g_{ds6}}$$ → that's quite large ∴ $\omega_p^- \gg \omega_p^+$

Thus, for an NMOS input op amp, PSRR⁻ is often better than PSRR⁺. → in design, need to worry more about PSRR⁺!

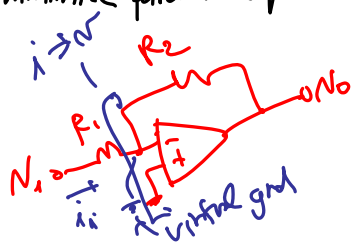
③ Some methods for reducing PSRR:

(i) Use buffer-based zero-cancellation in the compensation loop.

(ii) Use cascode circuitry, or balanced circuit topologies.

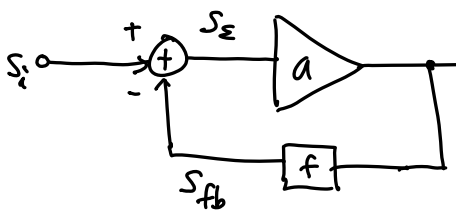
(iii) Supply-independent biasing.

(iv) Design strategies to minimize parasitic capacitive feedthrough.



Feedback

⇒ we know this:



$s_o = a s_\varepsilon$

$s_\varepsilon = s_i - f s_o$

⇓

$$\boxed{\frac{s_o}{s_i} = \frac{a}{1+af} = A}$$

Benefits of Negative FB

① Stabilizes the gain of the amp against parameter changes & active device variations

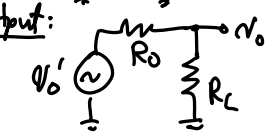
② Modifies R_i and R_o → basically improves their values according to the type of amplifier implemented

e.g., voltage amp: R_i: large, R_o: small

@ input:

If R_i: large, $v_i \approx v_s$. ($R_i \gg R_s$)

@ output:



If R_o: small, $v_o \approx v_o'$. ($R_o \ll R_L$)

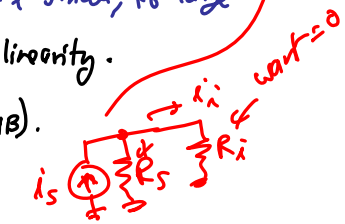
current-to-voltage amp: R_i: small, R_o: small

voltage-to-current amp: R_i: large, R_o: large

current-to-current amp: R_i: small, R_o: large

③ Reduces distortion; improves linearity.

④ Increases bandwidth (ω_{-3dB}).



Disadvantages of Neg. FB

① Gain is reduced → reduction factor ~ equal to the amount of gain stabilization, distortion reduction, etc...

Solution: Add more stages of gain → but this adds cost & power...

② Feedback causes stability problems (if not compensated properly)

Gain Sensitivity Reduction Via FB

$$A = \frac{a}{1+af} \rightarrow \frac{dA}{da} = \frac{(1+af) - af}{(1+af)^2} = \frac{1}{(1+af)^2}$$

For a Δ in op amp gain: δa

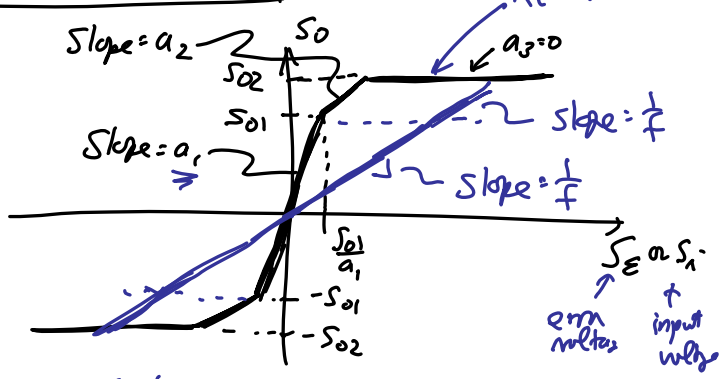
$$\frac{\delta A}{\delta a} = \frac{1}{(1+af)^2} \rightarrow \delta A = \frac{\delta a}{(1+af)^2}$$

much smaller than δa

... and the fractional change:

$$\frac{\delta A}{A} = \frac{1+af}{a}\frac{\delta a}{(1+af)^2} \Rightarrow \boxed{\frac{\delta A}{A} = \frac{\frac{\delta a}{a}}{1+af}}$$

Distortion Reduction via FB

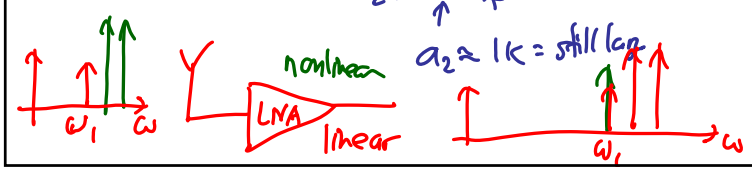


Now, close the loops

$0 < S_o < S_{o1}$: $A_1 = \frac{a_1}{1+a_1 f} \approx \frac{1}{f}$ for a_1 = large

$S_{o1} < S_o < S_{o2}$: $A_2 = \frac{a_2}{1+a_2 f} \approx \frac{1}{f}$

$a_2 \approx 1K$ = still large



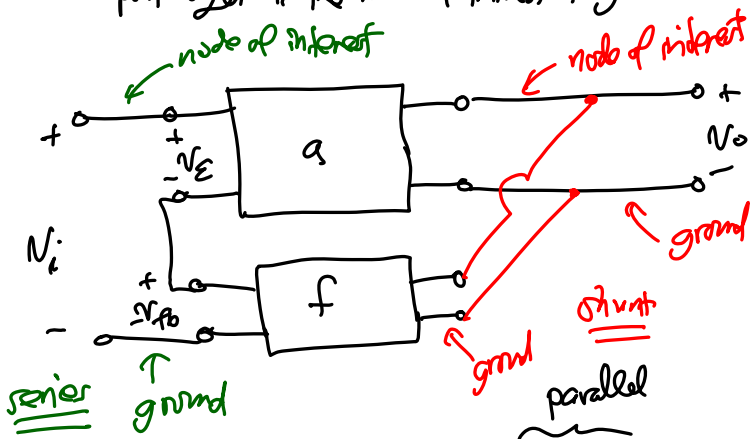
"Inspection" Analysis of FB Ckts.

↓ starts with...

Identification of FB Connection Types

Series Connection – FB network in series w/ the amplifier port

must go through both the FB port & the amplifier port to get f/ the node of interest to ground

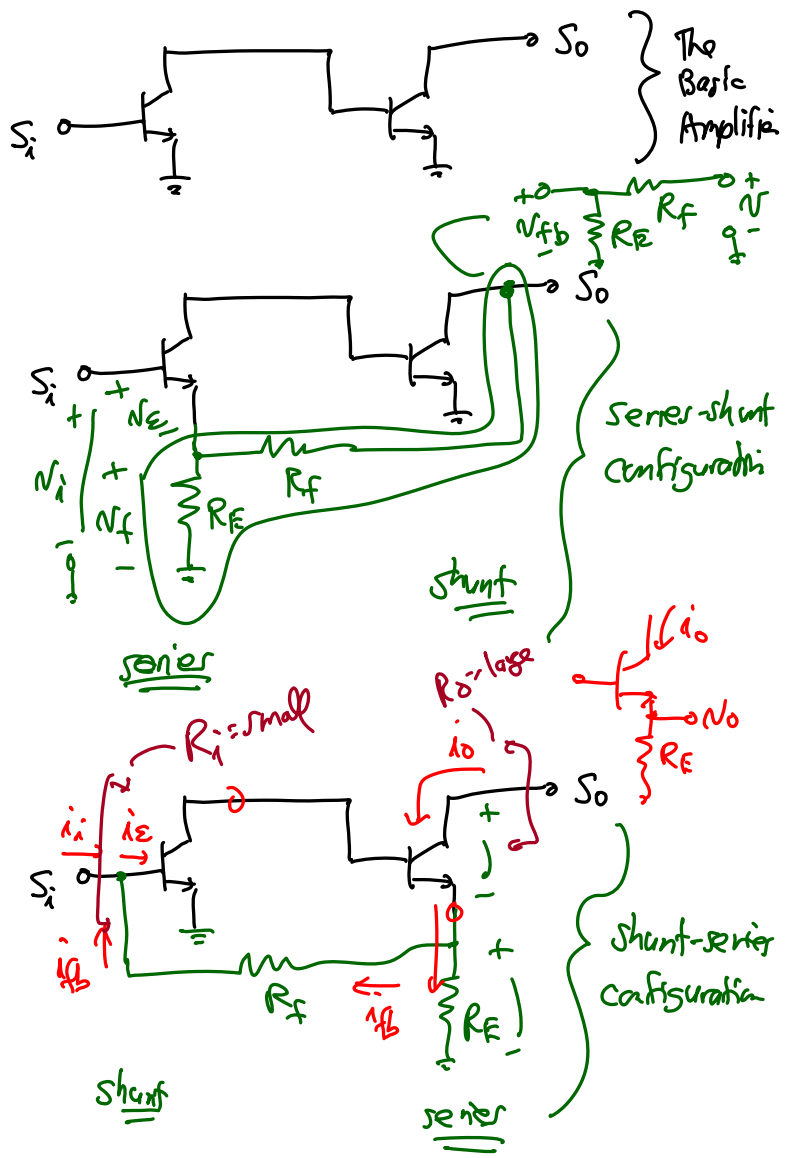


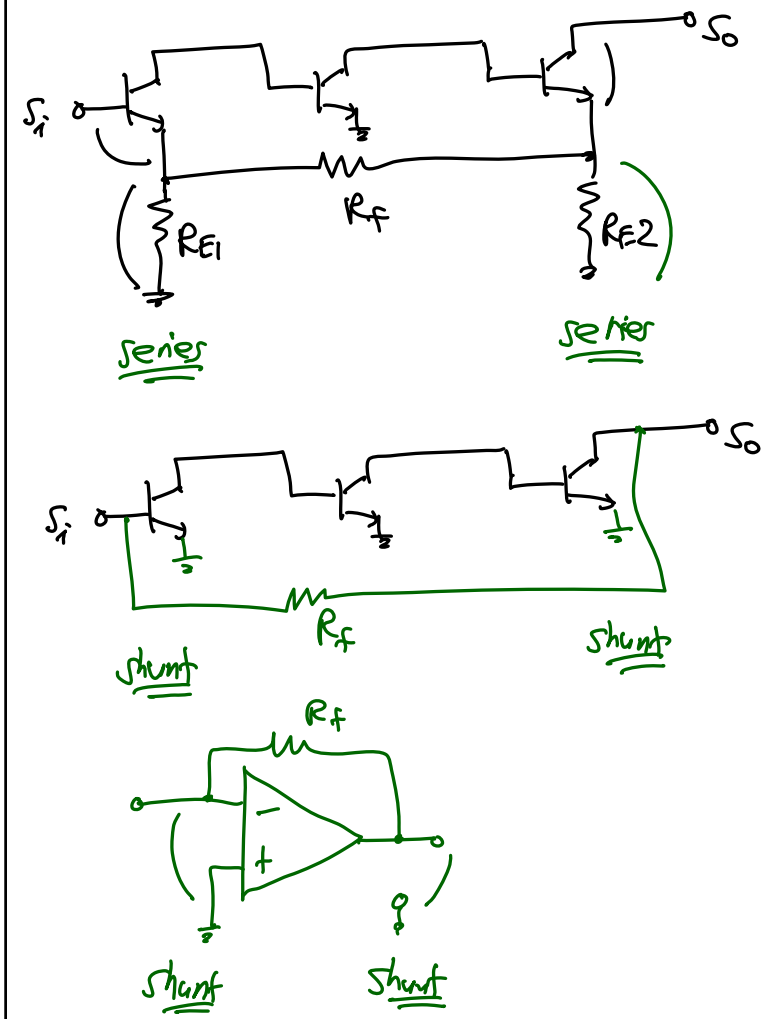
Shunt Connection: FB network port in shunt w/ the amplifier port

can get f/ the node of interest to ground via either FB network port or the amplifier port

series-shunt FB

Example.





⇒ from above → four different FB configurations.

Feedback Configurations

Input Variable	Input Connection	Output Connection	Output Variable
voltage	series	series	current
current	shunt	shunt	voltage

$v \to i$

$i \to v$

$i \to i$

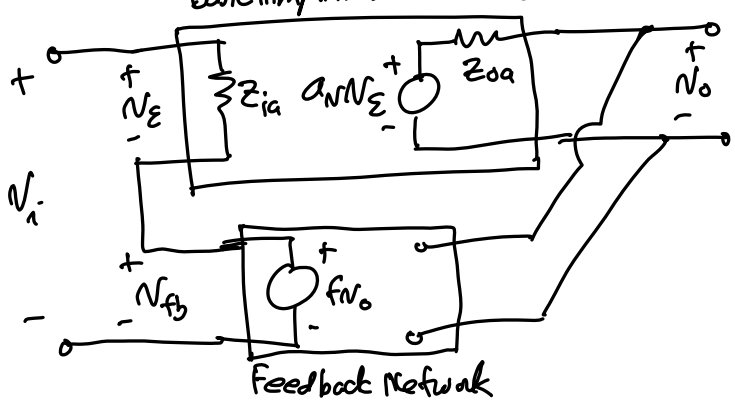
$v \to v$

Effect of FB on Z_i & Z_o

Ex: series-shunt FB

Assumption: FB network has ideal impedances
↳ i.e., it does not load the amplifier

Basic Amplifier: $v_\varepsilon \to v_o$



Find the T.F.:

$$\left.\begin{aligned} v_\varepsilon &= v_i - v_{fb} \\ v_o &= a_v v_\varepsilon \\ v_{fb} &= f v_o \end{aligned}\right\} \quad v_o = a_v(v_i - f v_o) \Rightarrow \boxed{\frac{v_o}{v_i} = \frac{a_v}{1 + a_v f}}$$

(as expected)