

PROBLEM SET #1

Issued: Tuesday, Jan. 24, 2012

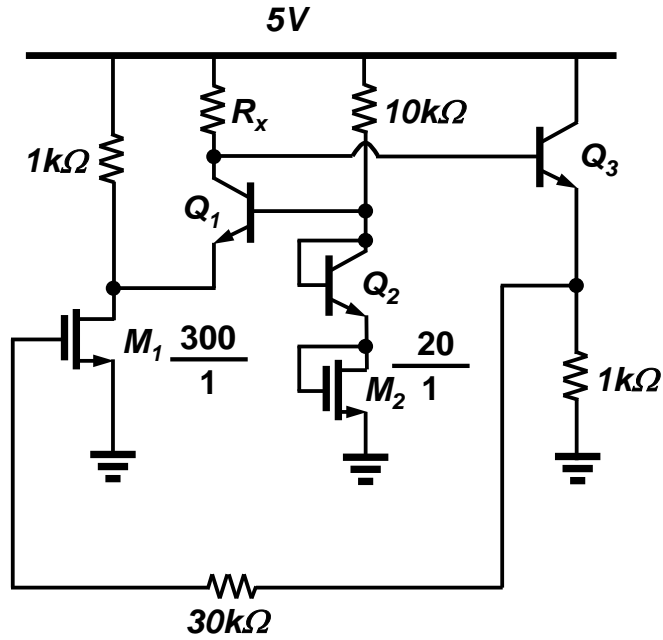
Due: Tuesday, Jan. 31, 2012, 5:00 p.m. in the EE 140 homework box in 240 Cory

1. Consider a *pn* junction diode in silicon with doping densities $N_A=10^{17}/\text{cm}^3$ and $N_D=10^{20}/\text{cm}^3$. (assume $n_i=10^{10}/\text{cm}^3$, junction area = $1\times 10^{-5}\text{cm}^2$)
 - (a) Calculate the built-in potential, depletion-layer depths and maximum field for a reverse bias of 5V.
 - (b) Repeat (a) for zero external bias and 0.3V forward bias.
 - (c) Calculate the junction capacitance at zero bias, 3V reverse bias and 0.5V forward bias.

2. Gray & Meyer, Chapter 1: Problem 1.9. (As in the text, assume $n_c=n_s=0.3$.)

3. An NMOS transistor has parameters $W=10\mu\text{m}$, $L=1\mu\text{m}$, $k'=200\mu\text{A}/\text{V}^2$, $\lambda=0.02\text{V}^{-1}$, $t_{ox}=100\text{\AA}$, $\phi_f=0.3\text{V}$, $V_{i0}=0.7\text{V}$, substrate doping concentration = $10^{15}/\text{cm}^3$, relative permittivity of Si = 11.8 and of gate oxide = 3.9. Ignore velocity saturation effects.
 - (a) Sketch the I_D - V_{DS} characteristics for V_{DS} from 0 to 3V and $V_{GS}=0.5\text{V}$, 1.5V, and 3V. Assume $V_{SB}=0\text{V}$.
 - (b) Sketch the I_D - V_{GS} characteristics for $V_{DS}=2\text{V}$ as V_{GS} varies from 0 to 2V with $V_{SB}=0\text{V}$, 0.5V, and 1V.
 - (c) Derive and sketch the *complete* small-signal equivalent circuit for the device with $V_{GS}=1\text{V}$, $V_{DS}=3\text{V}$ and $V_{SB}=1\text{V}$. Use $\psi_0=0.7\text{V}$, $C_{sb0}=C_{db0}=20\text{fF}$, and $C_{gb}=5\text{fF}$. Overlap capacitance from gate to source and gate to drain is 2fF.
 - (d) Under the bias condition in (c), calculate the frequency of unity current gain of this device.

4. Refer to the circuit shown below: ($\beta_f=100$, $V_A\rightarrow\infty$, $r_b=0$, $V_{BE(on)}=0.7\text{V}$, $V_{CE(sat)}=0.2\text{V}$, $k'=200\mu\text{A}/\text{V}^2$, $V_t=0.6\text{V}$, $\lambda=0$)
 - (a) Assume $R_x=10\text{k}\Omega$, calculate the DC operating points including the current flowing along each branch and DC voltage at each node. (You can assume $\beta_f\rightarrow\infty$ for part(a).)
 - (b) What is the maximum value for R_x that ensures all the BJT's are in forward active region?



5. Consider a bias circuit shown below. Calculate the output voltage V_{out} and output current I_{out} . Assume $V_{BE(on)}=0.7V$ and $V_{CE(sat)}=0.2V$.

