# PROBLEM SET #11

*Issued: Tuesday, Apr. 17, 2012*

*Due: Tuesday, Apr. 24, 2012*, 6:00 p.m. in the EE 140 homework box in 240 Cory

1. For the two-stage BiCMOS op amp shown in Fig. PS11.1, assume $V_{DD}$ = 1.2V, $C_L$ = 5pF, $I_{REF}$ = 20μA, and $(W/L)_7 = (W/L)_8$. Also, assume the output voltage $V_{out}$ is biased to 0V DC. The table below provides transistor parameter values. If necessary (and it might not be), determine any needed MOS capacitor values assuming lambda design rules.

| **MOS** | | | | |
|---|---|---|---|---|
| $\mu_p$=250cm$^2$/V-s | $V_{tp}$=-0.5V | $L_{drawn}$=1μm | $t_{ox}$=150Å | $\lambda$=0.1V$^{1/2}$ |
| $\psi_0$=0.7V | $n$=0.5 | $C_{j0}$=0.3fF/μm$^2$ | $C_{jsw0}$=2.2fF/μm | $C_{ol}$=0.18fF/μm$^2$ |
| **BJT** | | | | |
| $\beta_F$=100 | $V_A$=50V | $V_T$=26mV | $\tau_F$=20ns | $I_S$=10$^{-14}$A |
| $C_{je0}$=0.5pF | $C_{\mu 0}$=2pF | $C_{cs0}$=0.5pF | $\psi_{0s}$= $\psi_{0c}$=0.6V | $n_c$=$n_e$=0.5 |
| $V_{CE(sat)}$=0.2V | | | | |

Design values for the compensation capacitor $C_C$ and the sizes of each MOS transistor to satisfy the following specifications:

i. Unity-gain bandwidth ≥ 1MHz

ii. Phase margin ≥ 60° for unity-gain feedback

iii. Output swing ±1V

iv. Open-loop voltage gain ≥ 80dB

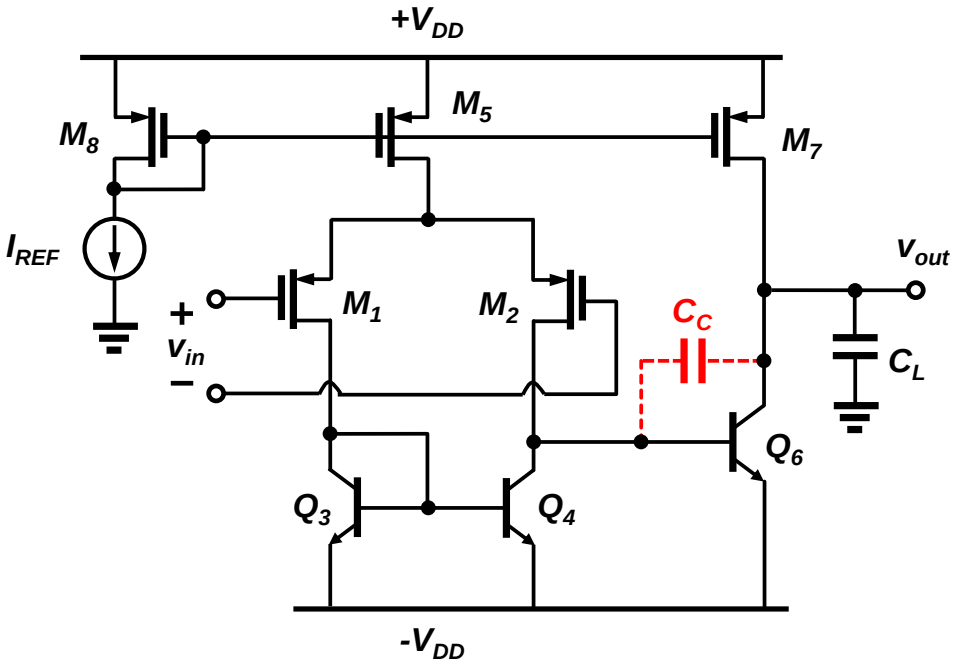


Fig. PS11.1