PROBLEM SET #12

Issued: Tuesday, Apr.24, 2012

Due: Tuesday,May.1, 2012, 6:00 p.m. in the EE 140 homework box in 240 Cory

1. Calculate the mid-band small-signal gain v_o/i_x, input resistance and output resistance of the amplifier shown in Fig. PS12.1. Use β_F = 150 and V_A = 50V.

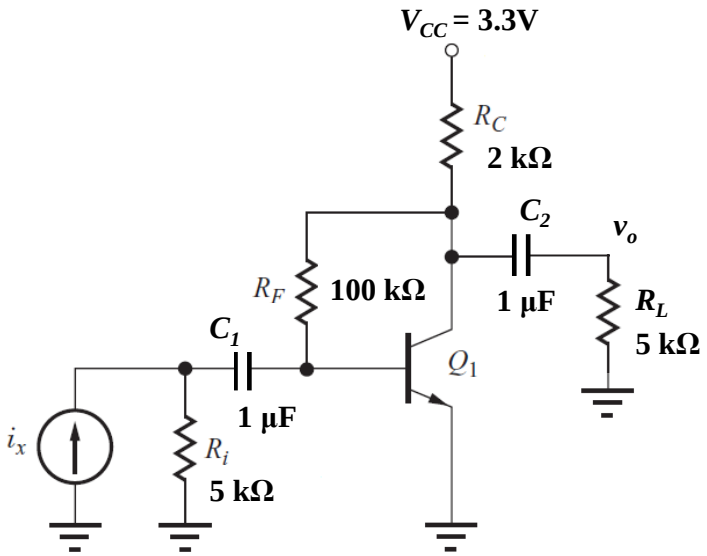

Fig. PS12.1

2. A variable-gain CMOS amplifier is shown in Fig. PS12.2. Note that M_4 represents shunt feedback around M_6. Assuming that the bias value of V_i is adjusted so that V_{GD6} = 0V dc, calculate the bias currents in all devices and the small-signal voltage gain and output resistance for V_c equal to 3 V, and then 4 V. Assume $\mu_p C_{ox}$ = 30μA/V^2, $\mu_n C_{ox}$ = 60μA/V^2, V_{tn} = $|V_{tp}|$ = 0.8V, $2\Phi_F$ = 0.6V, γ = 0.5V$^{1/2}$ and $\lambda_n = \lambda_p$ = 0.

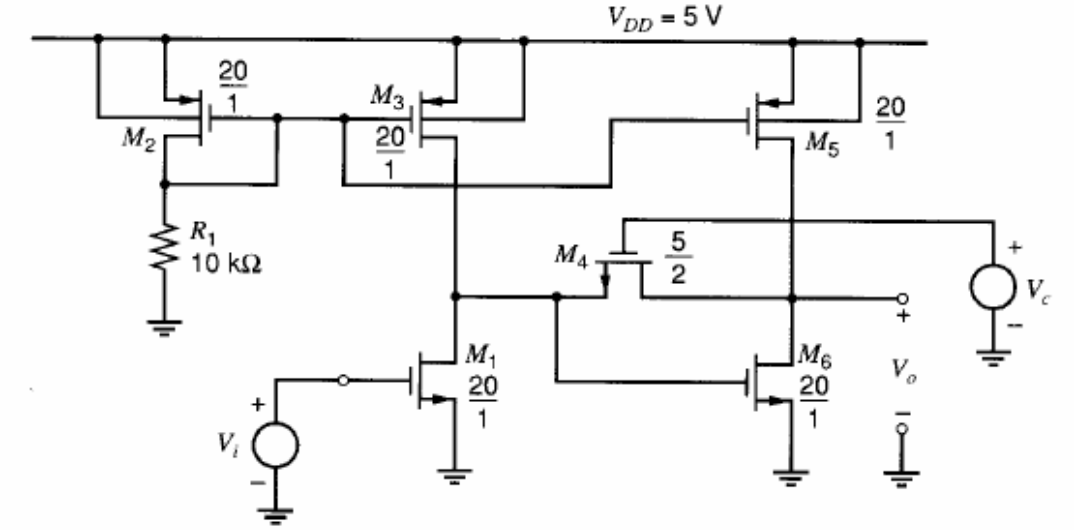

Fig. PS12.2

3. In the two CMOS amplifier circuits shown in Fig. PS12.3(a) and Fig. PS12.3(b), assume V_{tn} = 0.7V, V_{tp} = -0.8V, $\mu_n C_{ox}$ = 134.2μA/V^2, $\mu_p C_{ox} = \mu_n C_{ox}/3.5$, λ_n = 0.1V^{-1}, λ_p = 0.2V^{-1}. You can neglect body effect in this problem.

   (a) In the circuit of Fig. PS12.3(a), $(W/L)_{1\text{-}3}$ = 50μm/0.5μm, $I_{D1} = I_{D2} = I_{D3}$ = 0.5 mA, and $R_{S1} = R_F = R_{D2}$ = 3kΩ. Determine the input DC bias voltage V_{b1} required to establish the above currents, and then calculate the closed-loop voltage gain and output resistance.

   (b) The circuit in Fig. PS12.3(a) can be modified as shown in Fig. PS12.3(b), where a source follower, M_4, is inserted in the feedback loop. Note that M_1 and M_4 can also be viewed as a differential pair. Assume $(W/L)_{1\text{-}4}$ = 50μm/0.5μm, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$ = 0.5 mA, $R_{S1} = R_F = R_{D2}$ = 3kΩ, and V_{b2} = 1.5V. Calculate the closed-loop voltage gain and output resistance. Compare the results with those obtained in part (a).

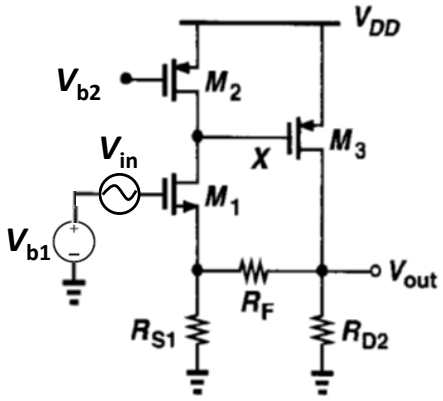

Fig. PS12.3 (a)

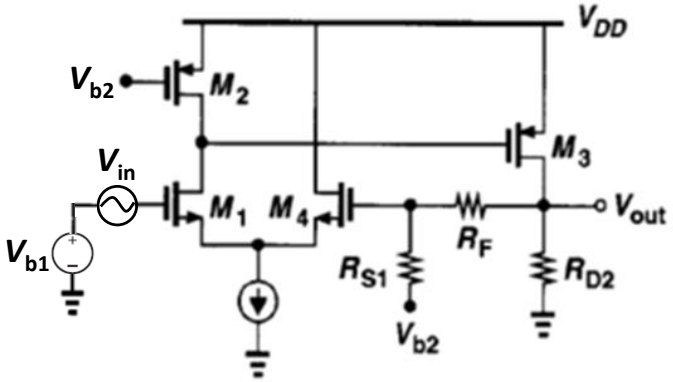

Fig. PS12.3 (b)