PROBLEM SET #8

Issued: Tuesday, Mar.13, 2012

Due: Tuesday, Mar.20, 2012, 6:00 p.m. in the EE 140 homework box in 240 Cory

1. In the circuit of Fig. PS8.1, assume $(W/L)_{1\text{-}4}$=100μm/0.5μm, $C_1 = C_2$ = 0.5 pF, I_{SS} = 1 mA, μ_n= 350 cm^2/V/s, μ_p= 100 cm^2/V/s, t_{ox} = 9nm, ε_r = 3.9, L_d = 0.08μm and $L_{eff} = L\text{-}2L_d$.

   (a) If a step voltage (as shown) is applied to the input of this circuit, find an expression for the time constant of its output response in terms of $g_{m1\text{-}4}$, $r_{o1\text{-}4}$, C_1 and C_2.

   (b) What is the slew rate of this circuit? With a 1-V step at the input, how long does it take for I_{D2} to reach $0.1I_{SS}$? Before I_{D2} reaches $0.1I_{SS}$, you can assume that the current through C_1 and C_2 roughly equals to I_{SS}.

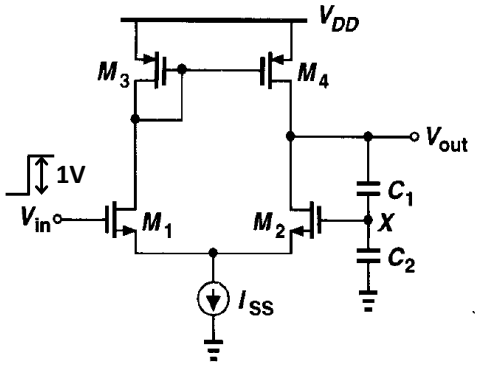

Fig. PS8.1

2. Fig. PS8.2 shows a multi-stage CMOS amplifier driving a capacitive load with value of C_L.

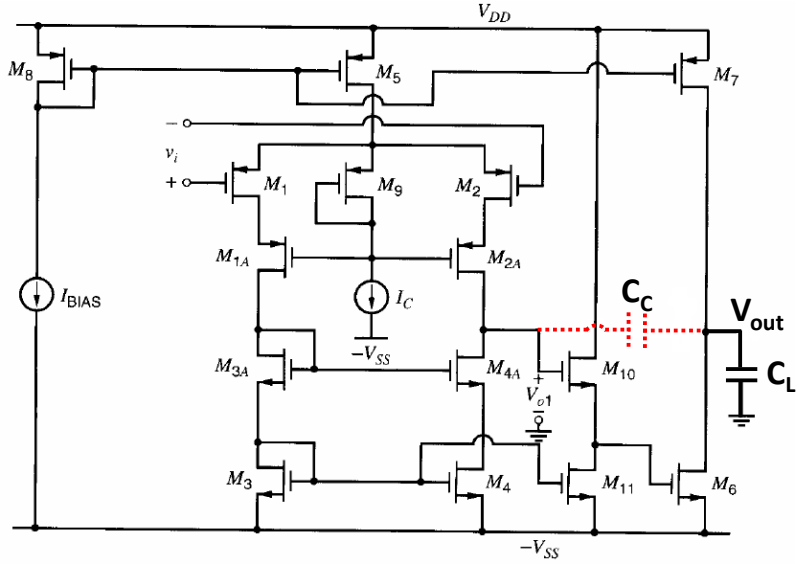

Fig. PS8.2

   (a) Determine the common-mode input range in terms of V_{DD} and V_{SS}. What is the minimum supply voltage difference that can satisfy this common-mode input range requirement?

Assume that all the transistors are enhancement-mode devices with $|V_t| = 1$ V, and ignore the body effect. Also assume that the biasing is arranged so that $|V_{ov}| = 0.2$ V for each transistor except M_9. Finally, assume that M_1 and M_2 are biased at the edge of the active region by M_9 and I_C.

(b) Determine an expression for the -3dB bandwidth of the circuit in terms of C_L, I_{bias}, I_c, λ_p, λ_n. Assume that the pole at the output node is the dominant pole and ignore all other capacitances except C_L.

(c) Now the load capacitor C_L is replaced by a capacitor C_C between M_{4A} drain and the output node (as shown with red dashed line in Fig. PS8.2). Determine an expression for C_C that can keep the same -3dB bandwidth as you calculated in part (b).

3. In this problem, we design a two-stage op amp based on the topology shown in Fig. PS8.3. Assume a power budget of 6 mW, a required output swing of 2.5 V, and a power supply V_{DD}=3V. For all devices, L_{eff} = 0.5 μm, μ_n= 350cm^2/V/s, μ_p= 100cm^2/V/s, λ_n=0.1 V^{-1}, λ_p=0.2 V^{-1}, C_{ox}=3.836fF/μm^2. $|V_{THp}| = 0.8$ V, $|V_{THn}| = 0.7$ V. You can neglect the body effect.

(a) Allocating a current of 1mA to the output stage and roughly equal overdrive voltages to M_5 and M_6, determine $(W/L)_5$ and $(W/L)_6$. Note that the gate-source capacitance of M_5 is in the signal path whereas that of M_6 is not. Thus, M_6 can be quite a bit larger than M_5.

(b) Calculate the small-signal gain of the second stage.

(c) With the remaining 1 mA flowing through M_7, determine the aspect ratio of M_3 (and M_4) such that $V_{GS3} = V_{GS5}$. This is to guarantee that if $V_{in} = 0$ and hence $V_X = V_Y$, then M_5 carries the expected current.

(d) Calculate the aspect ratios of M_1 and M_2 such that the overall voltage gain of the op amp equals to 500.

(e) Identify the positive and negative input of the circuit and connect this op amp in unity-gain feedback.

(f) What is the allowable input voltage range? Assume $|V_{GS7}-V_{TH7}| = 0.4$ V.

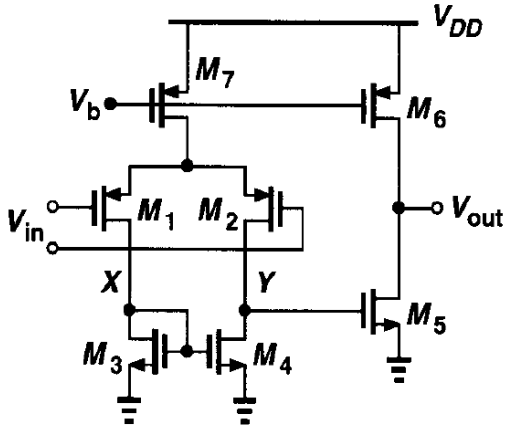

Fig. PS8.3

4. Fig. PS8.4(a) shows the input stage and second stage schematic of the classic μA741 operational amplifier. Assume V_{CC}=V_{EE}=15 V, $\eta_{npn}=2\times10^{-4}$, $\eta_{pnp}=5\times10^{-4}$, β_{F0} = 250 and $I_S=1\times10^{-14}$A.
   (a) For the op amp bias circuit shown in Fig. PS8.4(b), calculate I_{REF}, I_2 and I_1. You can assume $\beta = \infty$ and $V_A = \infty$ for transistor $Q_{10\text{-}13}$ in this part.
   (b) Calculate the overall small signal voltage gain of this op amp.

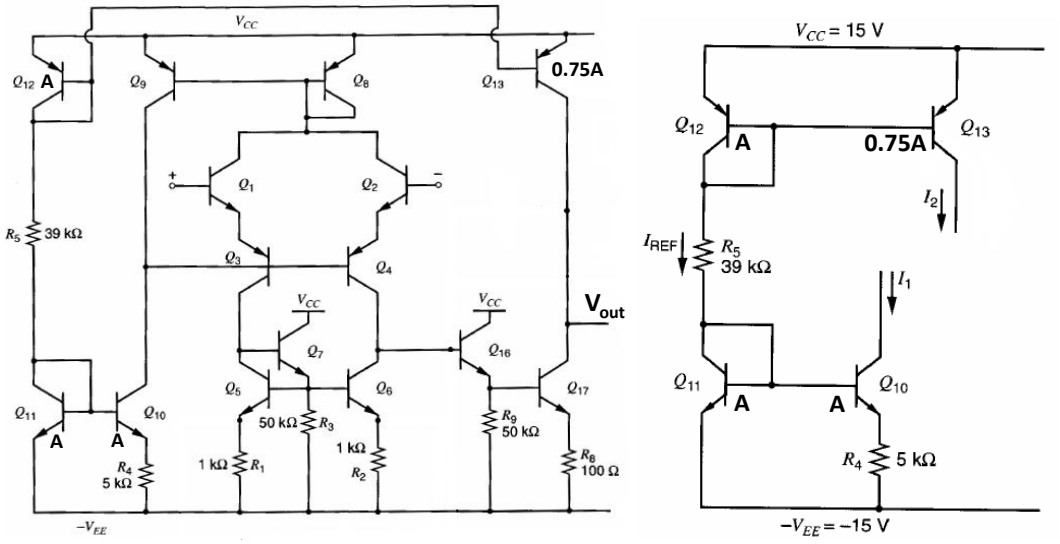

Fig. PS8.4