PROBLEM SET #9

Issued: Tuesday, Apr. 3, 2012

Due: Tuesday, Apr. 10, 2012, 6:00 p.m. in the EE 140 homework box in 240 Cory

1. Consider a class B output stage depicted in Fig. PS9.1(a). Assume V_{CC} = 10V, and both transistors have the same $|V_{th}|$ = 1V and $\mu C_{OX}W/L$ = 200μA/V^2.
   (a) Assuming the input is fed with a sine-wave signal with a 5-V amplitude (i.e., V_{in} = 5sin(ωt)) and $R_L \rightarrow \infty$, sketch the output voltage waveform.
   (b) (Continuing from part (a)) For what value of load resistor R_L is the peak output voltage reduced to half of the input signal amplitude (i.e., $|V_{out,peak}|$ = 2.5V)?
   (c) The class B output stage is connected with an op amp into a feedback configuration as shown in Fig. PS9.1(b). The op amp has an open loop voltage gain A_0 = 100 V/V. Sketch the transfer characteristic v_{out} vs. v_{in}. Assume $R_L \rightarrow \infty$.
   (d) (Continuing from part (c)) The 5-V-amplitude input signal is now connected to the input of the circuit in Fig. PS9.1(b). Assuming the op amp has a slew rate of 10V/μS, calculate the maximum allowable frequency of the input signal for the output waveform NOT having distortion due to slew rate limitation.

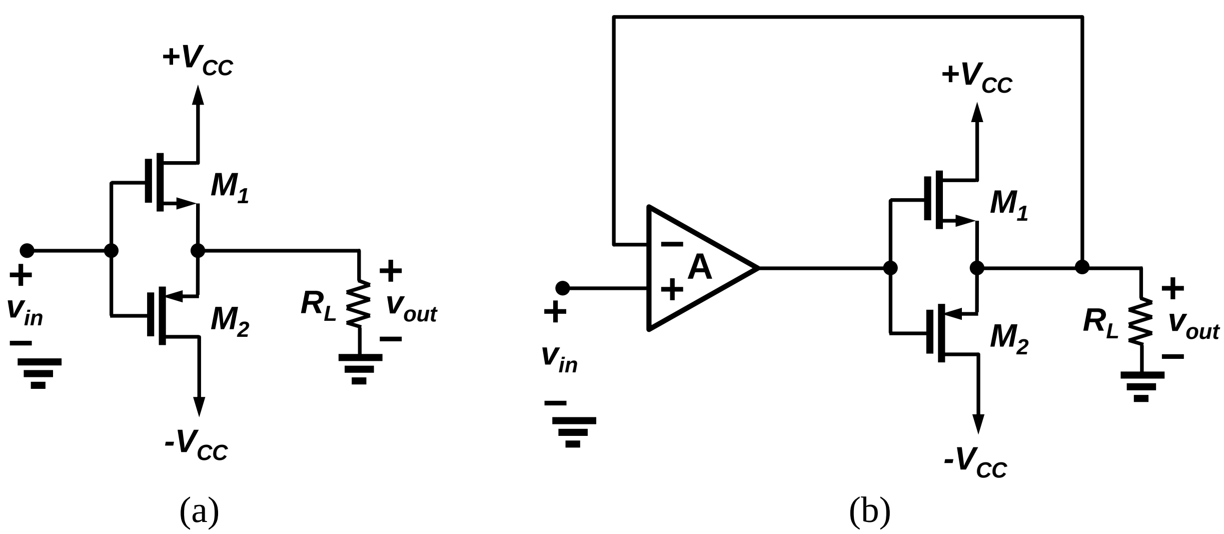

Fig. PS9.1

2. In the circuit of Fig. PS9.2, V_{CC} = 20V, I_Q = 0.1mA, R_L = 1kΩ, and for all devices β_F = 150, I_S = 10^{-15}A, V_T = 26mV, and $|V_{CEsat}|$ = 0.2V.
   (a) Calculate the value of V_{in} and the current in each device for V_{out} = 0, ±5V, and ±10V. Then sketch the transfer characteristic of V_{out} vs. V_{in} from V_{out} = 10V to -10V.
   (b) Calculate the largest possible positive and negative output signal levels.

(c) Suppose that you want to achieve a positive peak level equal to the negative peak output level for this circuit by adjusting the I_Q value. What value of I_Q is required to achieve this?

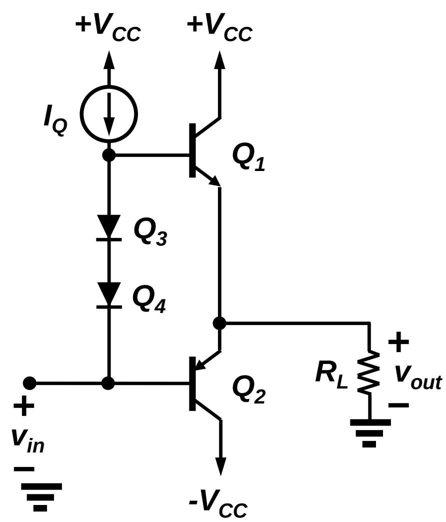

Fig. PS9.2

3. In the amplifier of Fig. PS9.3, assume $\mu_n C_{OX} = 2\mu_p C_{OX} = 200\mu A/V^2$, $\lambda_p = 2\lambda_n = 0.2$, $(W/L)_{1\text{-}4} = 50/0.5$ and $I_{SS} = I_1 = 1mA$.
   (a) Assuming $C_X = C_Y = 0.5pF$, estimate the poles at nodes X and Y, and the phase margin for unity-gain feedback.
   (b) If $C_X = 1pF$, estimate the maximum tolerable value of C_Y that yields a phase margin of 60° for unity-gain feedback.

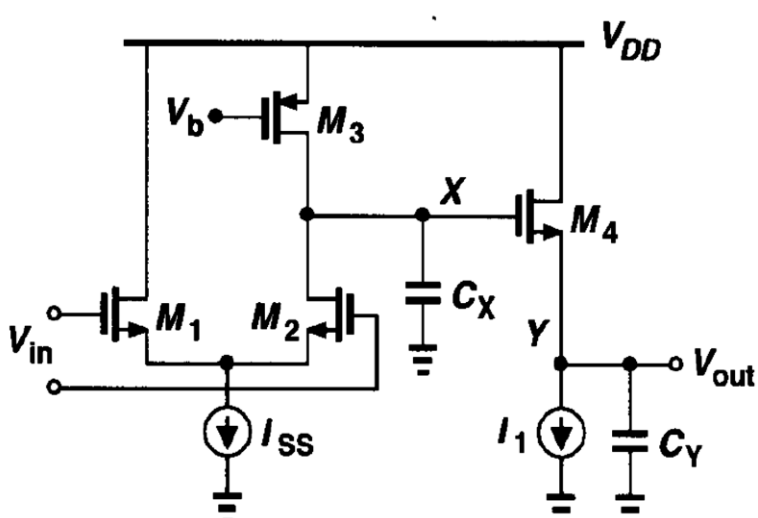

Fig. PS9.3

4. An amplifier has a low-frequency forward gain of 5000 and its transfer function has three negative real poles with magnitudes 300kHz, 2MHz, and 25MHz.
   (a) Suppose the amplifier is to be compensated by reducing the magnitude of the most dominant pole and assume the remaining poles do not move. Calculate the dominant-pole magnitude required for unity-gain compensation with 60° phase margin, and the corresponding bandwidth of the circuit with the feedback applied.
   (b) Repeat (a) for compensation in a feedback loop with a closed-loop gain of 20dB and 60° phase margin.

5. An op amp having a low-frequency gain of 1000 and a single pole roll-off at 10^4rad/s is connected in a negative-feedback loop via a feedback network having a transmission *k* and a two-pole roll-off also at 10^4rad/s. Find the critical value of *k* at which oscillation will occur.