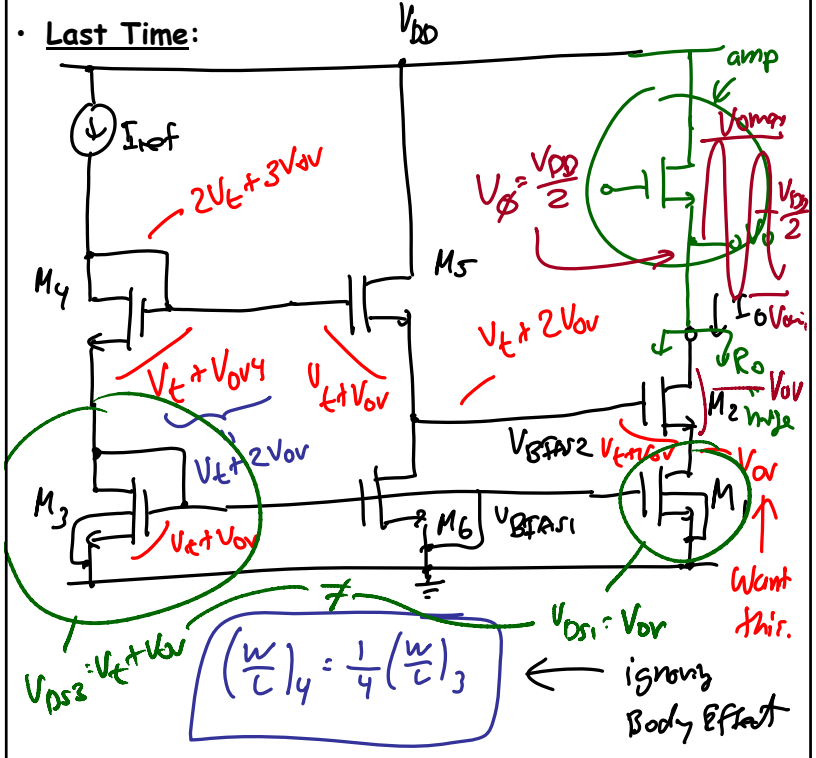
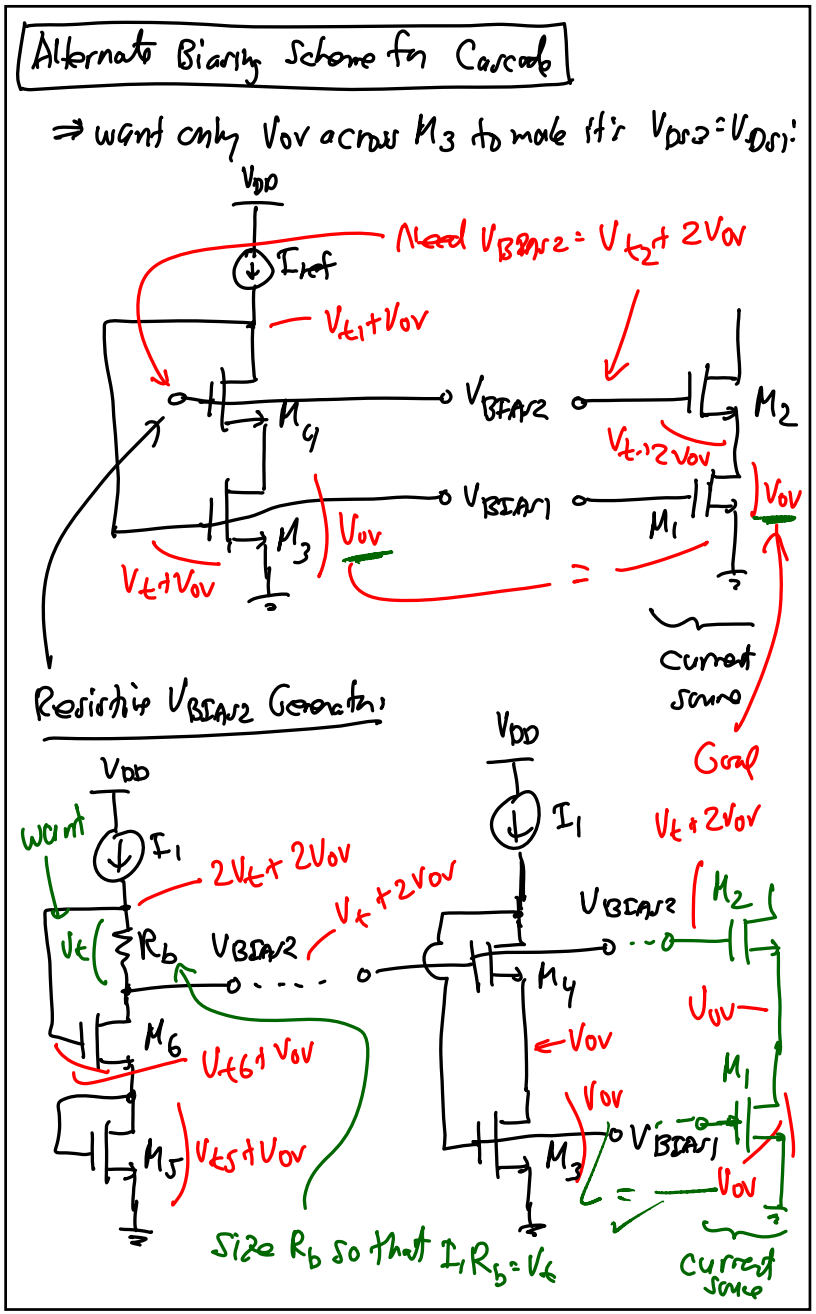
Lecture 11: Current Source Matching

- Announcements:
  - HW#4 due today at 6 p.m. in the EE140 drop box
  - HW#5 online
  - Lab#2 starts this week
- Lecture Topics:
  - High Swing Current Sources (cont.)
  - Current Source Matching Considerations
  - Op Amp Review
- ----------
- Last Time:





Issues:

① I_1R_b not all that well-controlled.

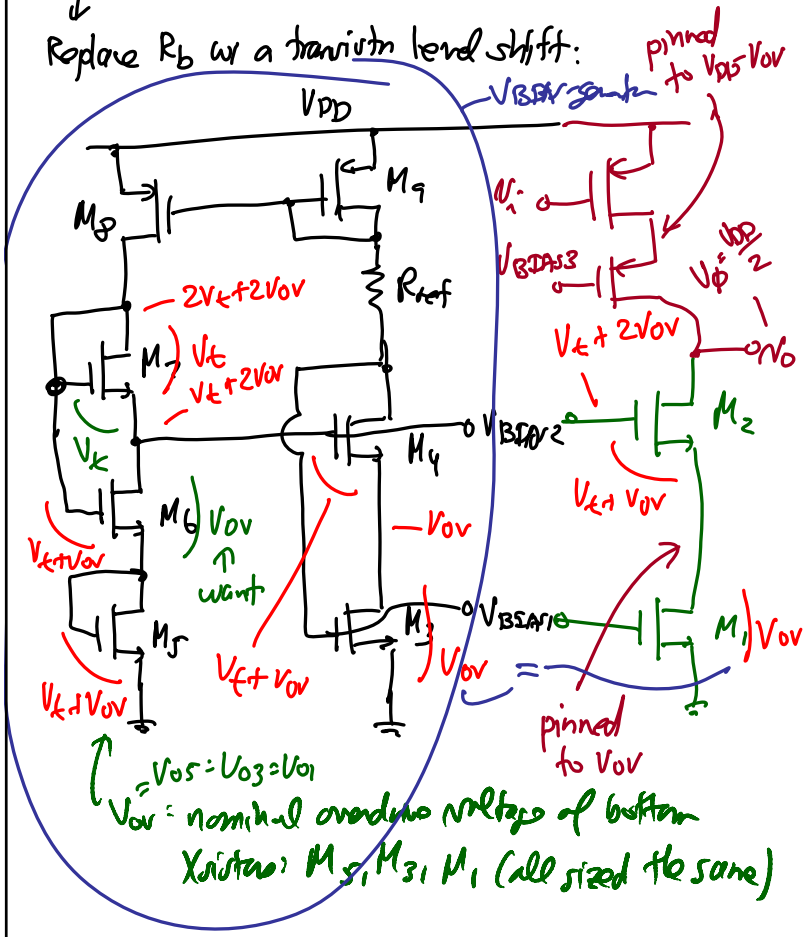
② Resistor = area consumption.

③ Body effect complicates things:

↳ really need: $I_1R_b = V_{t5} + V_{t6} - V_{t4}$

↓

Replace R_b w/ a transistor level shifter:



Design:

Demand that all transistors are saturated.

Approach 1: Want $V_{GS7} = V_{t1}$, so must make $\left(\frac{W}{L}\right)_7$ large, so that:

$$V_{OV7} = \sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_7}} \to 0, \text{ then}$$

↓

Problem: too much chip area!

Solution ↓

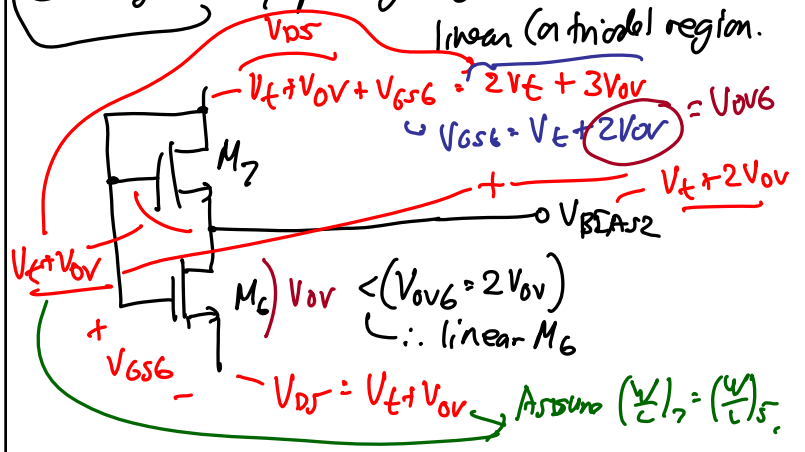
Approach 2: → recognize that devices in the V_{BIAS}-generation don't all need to be saturated → some can be linear!

① Allow M_7 to drop $V_{GS7} = V_t + V_{OV}$

② Still need $V_{DS6} = V_{OV} = V_{OV5} = V_{OV7}$ (assume M_5 & M_7 are same size)

↓

③ Can get this by operating M_6 in the linear (or triode) region.



Get size of M_6:

$I_{D7} = I_{D6}$

Saturated M_7: $I_{D7} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_7 (V_{GS7}-V_t)^2$ ($V_{GS7}-V_t = V_{ov}$)

Linear M_6: $I_{D6} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_6 \left[2(V_{GS6}-V_t)V_{DS6} - V_{DS6}^2\right]$ ($V_{GS6}-V_t = 2V_{ov}$, $V_{DS6} = V_{ov}$)

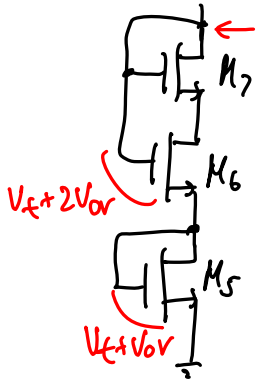
$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_7 (V_{ov})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_6 \left[2(2V_{ov})^2 V_{ov} - (V_{ov})^2\right]$$

$$\left(\frac{W}{L}\right)_7 = 3\left(\frac{W}{L}\right)_6$$

$$\left(\frac{W}{L}\right)_6 = \frac{1}{3}\left(\frac{W}{L}\right)_7 \text{ \& all other } \frac{W}{L}\text{'s} = \left(\frac{W}{L}\right)_7$$

→ Allows $V_{DS3} = V_{DS1}$ ∴ $I_O = I_{ref}$!

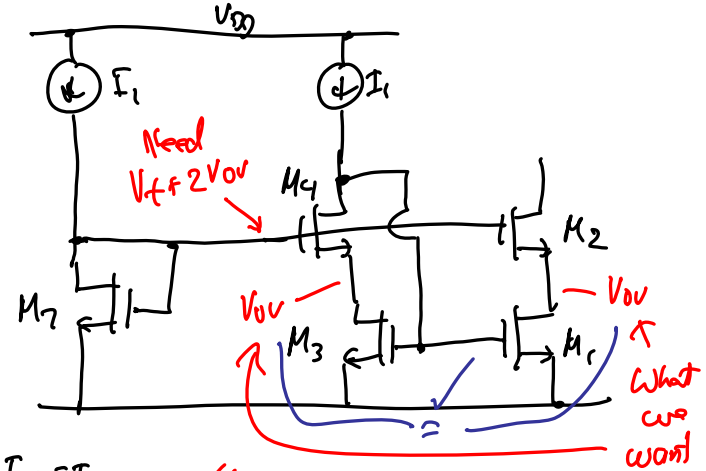
But Problem: We're using too much voltage to do this!



← $2V_t+3V_{ov} = 2(0.7)+3(0.3) = 2.3V$!

Too much! (in a 2V supply!)

Too much voltage? Can fix as follows:



$I_{D7} = I_{D3}$

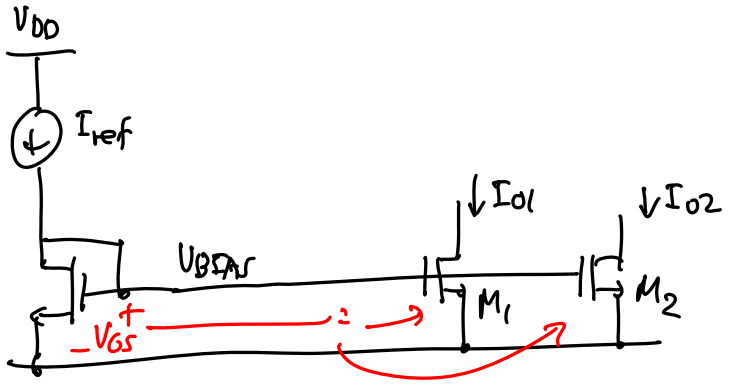
$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_7 (2V_{ov})^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 (V_{ov})^2$$

$$\therefore \left(\frac{W}{L}\right)_7 = \frac{1}{4}\left(\frac{W}{L}\right)_3 = \frac{1}{4}\left(\frac{W}{L}\right)_{\text{rest}}$$

↑ rest of the transistors

Note: Still must worry about Body effect!
↳ design defensively...
↳ Make $V_{DS7} > V_t + 2V_{ov}$

Current Source Matching Considerations



In MOS, we often need matched current sources:

$I_{D1} : I_{D2} \rightarrow I_{D1} = I_{D2}$

$I_{D1} = I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{t1})^2$

$I_{D2} = I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS1} - V_{t2})^2$

These can't be perfectly matched if

$(W/L)_1 \neq (W/L)_2$ & $V_{t1} \neq V_{t2}$

will always have this due to finite fabrication tolerances.

How do we quantify the degree of mismatch in I_D or I_D between current sources? → want $\frac{\Delta I_D}{I_D}$

Define average & mismatch quantities:

Average	Mismatch
$I_D = \frac{1}{2}[I_{D1} + I_{D2}]$	$\Delta I_D = I_{D1} - I_{D2}$
$\frac{W}{L} = \frac{1}{2}\left[\left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2\right]$	$\Delta\left(\frac{W}{L}\right) = \left(\frac{W}{L}\right)_1 - \left(\frac{W}{L}\right)_2$
$V_t = \frac{1}{2}[V_{t1} + V_{t2}]$	$\Delta V_t = V_{t1} - V_{t2}$

$\frac{\Delta I_D}{I_D}$ ≙ fractional current mismatch

$\frac{\Delta(W/L)}{(W/L)}$ ≙ fractional (W/L) mismatch

$\frac{\Delta V_t}{V_t}$ ≙ " V_t "

Rearranging:

$I_{D1} = I_D + \frac{\Delta I_D}{2}$ $\quad \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right) + \frac{\Delta(W/L)}{2}$ $\quad V_{t1} = V_t + \frac{\Delta V_t}{2}$

$I_{D2} = I_D - \frac{\Delta I_D}{2}$ $\quad \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right) - \frac{(W/L)}{2}$ $\quad V_{t2} = V_t - \frac{\Delta V_t}{2}$

Plug these into the current equations:

$$I_{D1} = I_D + \frac{\Delta I_D}{2}\left(\frac{W}{L}\right)_1 \quad \& \quad I_{D2} = I_D - \frac{\Delta I_D}{2}\left(\frac{W}{L}\right)_2$$

$$= \frac{1}{2}\mu_n C_{ox}\left[\left(\frac{W}{L}\right) + \frac{\Delta(W/L)}{2}\right]\left[V_{GS} - V_t - \frac{\Delta V_t}{2}\right]^2$$

(V_{ov}; $-V_{t1}$; neg!)

$$= \frac{1}{2}\mu_n C_{ox}\left[(W/L) + \frac{\Delta(W/L)}{2}\right]\left[V_{ov}^2 - 2V_{ov}\frac{\Delta V_t}{2} + \frac{(\Delta V_t)^2}{4}\right]$$

$$= \frac{1}{2}\mu_n C_{ox}\left[(W/L)V_{ov}^2 + \frac{\Delta(W/L)}{2}V_{ov}^2 - (W/L)V_{ov}\Delta V_t - \frac{\Delta(W/L)}{2}V_{ov}\Delta V_t\right]$$

(neg!)

$$= \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{ov}^2 + \frac{1}{2}\mu_n C_{ox}V_{ov}^2\left[\frac{\Delta(W/L)}{2} - \frac{(W/L)}{V_{ov}}\Delta V_t\right]$$

(I_D; I_D; fractional $\left(\frac{W}{L}\right)$)

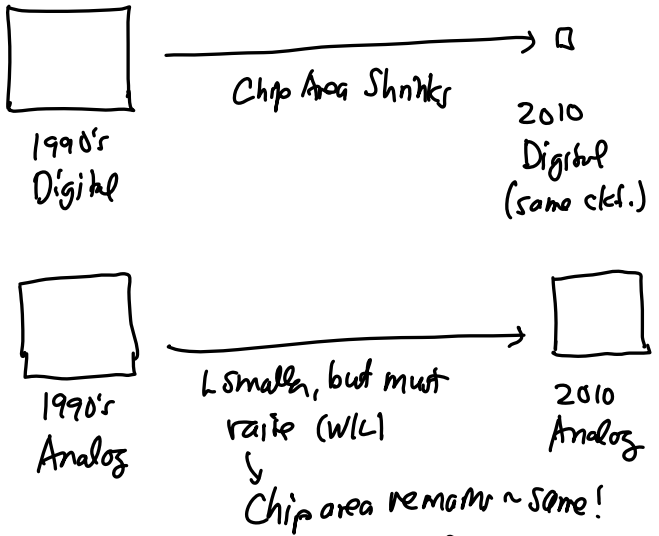
$$\frac{\Delta I_D}{2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)V_{ov}^2\left[\frac{1}{2}\frac{\Delta(W/L)}{(W/L)} - \frac{\Delta V_t}{V_{ov}}\right]$$

$$\therefore \frac{\Delta I_D}{I_D} = \frac{\Delta(W/L)}{(W/L)} - \frac{\Delta V_t}{(V_{ov}/2)}$$

this could be (-), so this doesn't necessarily help!

- Fractional Current Mismatch
- Geometry Based Component ← helps
  - ↑ Independent of Bias Pt.
- Increases as V_{ov} ↓
  - Today: V_{DD} ↓ → V_{ov} ↓
  - For each new Xistr generation, must make $\left(\frac{W}{L}\right)$ ↑

For analog dctr, when V_{DD} ↓ → V_{ov} ↓ → must make $\left(\frac{W}{L}\right)$ ↑ to counteract → this means analog dctr. generally don't get smaller as gates get shorter



⇒ analog dctr. benefit much less from scaling