

These diodes set this voltage

very important!

$\omega_H = \frac{1}{RO_C_L}$

all caps. @ this node, including from the next stage

This contributor the dominant pole:

Problems/Issues:

① Limited output swing

$$V_{omax} = V_{DD} - |V_{E7}| - |V_{OV7}| - |V_{E5}| - |V_{OV5}| + |V_{E6}| + |V_{OV6}| - |V_{OV6}|$$

Problem: Not enough swing!

$$V_{omin} = V_{OV5} + V_{OV2} + V_{OV4}$$

overdrive voltage of the tail current source

$$V_{swing} = V_{omax} - V_{omin}$$

Problem ②: Difficult to tie input to output!

Unity gain buffer (very useful!)

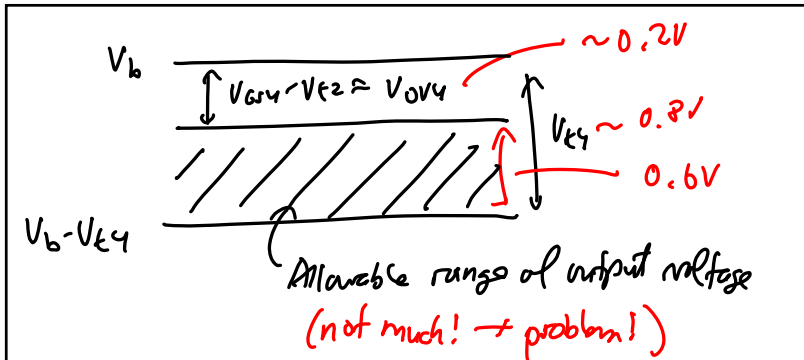
Comes from $V_{OV5} + V_{OV4} - V_{OV6}$

Want to know what range of V_{out} keeps all devices saturated?

Must keep $M4$ & $M5$ saturated!

$M4$: Need $V_{out} \geq V_b - V_{GS4} + V_{OV4} = V_b - V_{E4} - V_{OV4} + V_{OV4}$
 $\therefore V_{out} \geq V_b - V_{E4}$

$M2$: Need $V_{out} \leq V_x - V_{OV2} + V_{E2} + V_{OV2}$
 $V_{out} \leq V_b - V_{E4} - V_{OV4} + V_{E2} \approx V_b - V_{OV4}$
 $V_{E2} \approx V_{E4}$



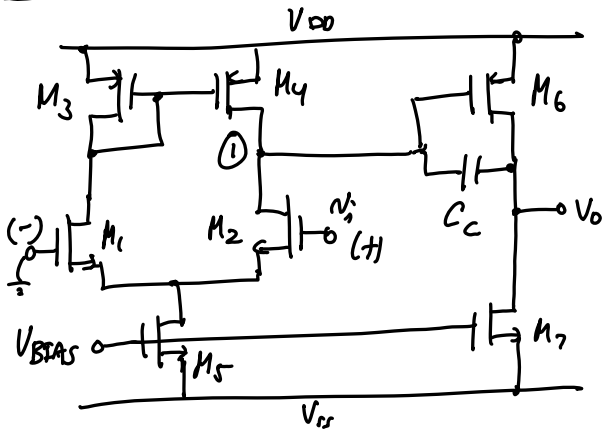
Problem 3:

Low freq. non-dominant pole associated w/ the "mirror" node → will hurt stability in feedback ctr.!
(we'll cover this later)

Soln: fully-differential, fully balanced

Another solution: 2-stage op amp

Classic 2-stage Op Amp



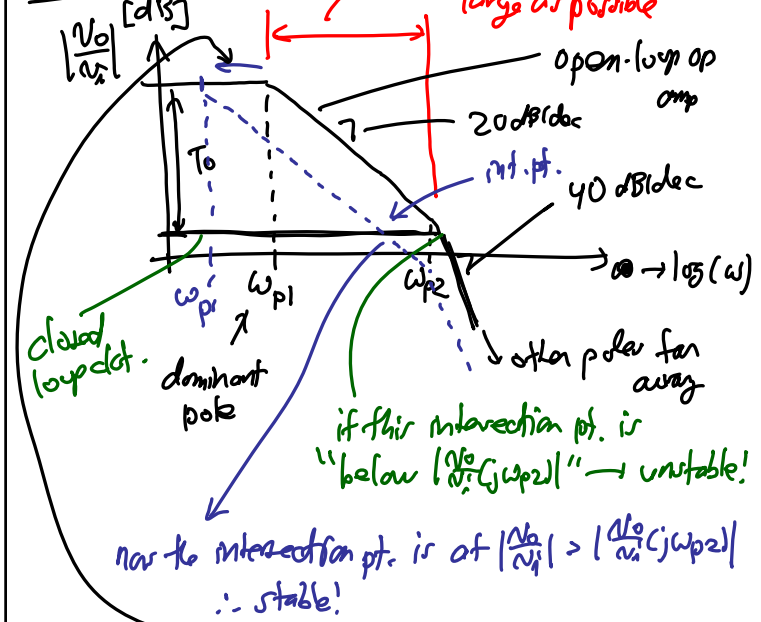
Gain-

1st stage: $A_{v1} = \frac{V_{o1}}{V_i} = -g_{m2}(r_{o2} || r_{o4})$

2nd stage: $A_{v2} = \frac{V_o}{V_{o1}} = -g_{m6}(r_{o6} || r_{o7})$

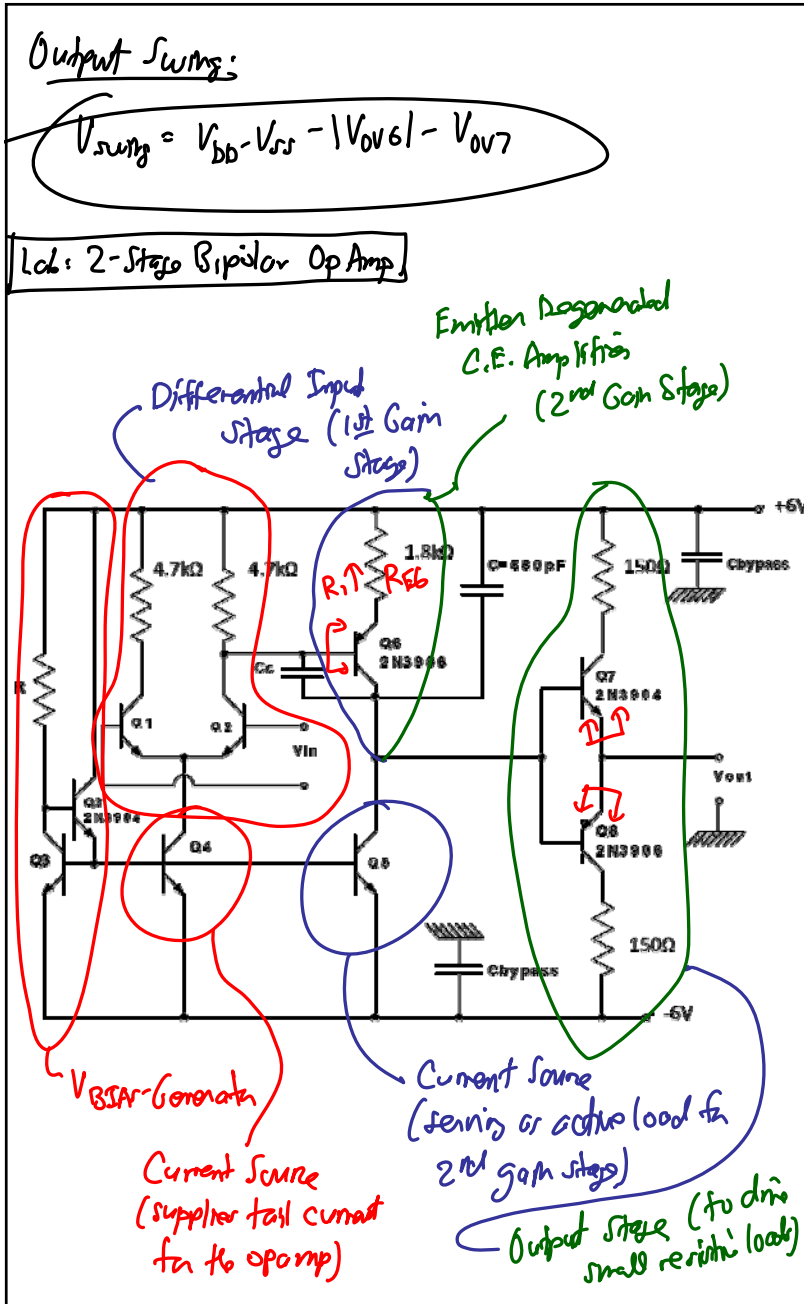
$A_v = A_{v1} A_{v2} = g_{m2}(r_{o2} || r_{o4}) g_{m6}(r_{o6} || r_{o7})$

Freq. Response:



Dominant Pole:

$\omega_{p1} = \omega_H = \frac{1}{(r_{o2} || r_{o4})(1 + g_{m6}(r_{o6} || r_{o7}))C_c}$
 Miller Effect



Remarks:

- ① You analyze this in Lab#2.
- ② Usually, the resistively-loaded diff. pair is replaced w/ an active current mirror load for more gain.
- ③ R_{E6} raises the input R of Q_6 (of the 2nd gain stage), plus helps w/ biasing.
- ④ Same comment as ③ for the output stage.
- ⑤ Output stage needed when driving a resistive load

↳ often the case for bipolar

↳ not often the case for MOS, where a capacitive load C_L is often more relevant → MOS op amps often don't need output stages!

