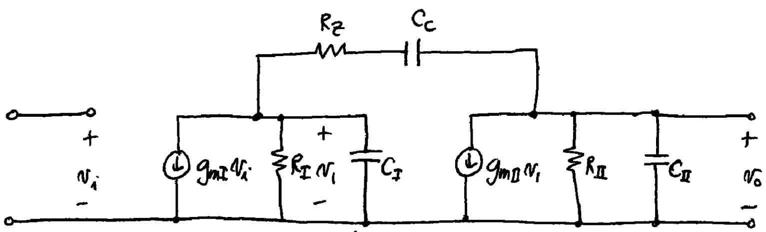
## Lecture 24: Slew Rate, Settling Time, & PSRR

- Announcements:
- Hutton online
- Design Project Checkpoint:
  - Due Monday, April 23, 11:59 p.m.
  - Send to your TA a spice file for your op amp design that simulates correctly, i.e., that reaches a stable bias point where all transistors are saturated (or linear if an MOS resistor)
  - It doesn't need to meet the project specs, but it should simulate correctly
- Lecture Topics:
  - Nulling the RHP Zero (finish compensation)
  - Slew Rate (revisited)
  - Settling Time
  - Power Supply Rejection Ratio (PSRR)
- ---------------------------------------
- Last Time:

**Nulling Resistor in Series w/ $C_C$**




Doing KCL: $p_1 \cong -\frac{1}{g_{mII}R_IR_{II}C_c}$

$p_2 \cong \frac{-g_{mII}C_c}{C_IC_{II}+C_c(C_I+C_{II})}$ } Same as before

$p_3 = -\frac{1}{R_ZC_I}$ ← pole due to $R_Z$

$z_1 = \frac{1}{C_c\left(\frac{1}{g_{mII}}-R_Z\right)}$ ← relocated zero (function of $R_Z$)

**Zero Placement Strategies**

① Eliminate $z_1$ → move it to ∞:

$z_1 = \frac{1}{C_c\left(\frac{1}{g_{mII}}-R_Z\right)} \to \infty$ when $\boxed{R_Z = \frac{1}{g_{mII}}}$

→ After doing this: $p_3 \cong -\frac{g_{mII}}{C_I}$, $p_2 \cong -\frac{g_{mII}}{C_{II}}$ } Usually, $C_{II} \gg C_{I}$, since $C_{II} = C_L$.

→ so these poles are often very far apart. (but be careful)

↓

This is good... but we could do better...

② Eliminate $p_3$ by placing $z_1$ on top of it:

$z_1 = p_3 = \frac{1}{C_c\left(\frac{1}{g_{mII}}-R_Z\right)} = -\frac{1}{R_ZC_I}$

↓

$$\boxed{R_Z = \frac{1}{g_{mII}\left(1-\frac{C_I}{C_c}\right)}}$$

After this:

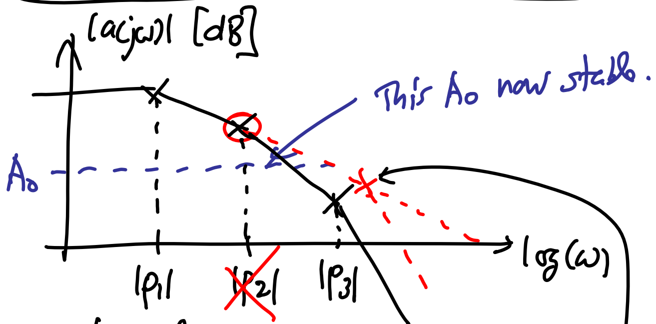
① $p_3$ gone; $p_1$ & $p_2$ left

② Now, can place $\omega_{u1t}$ @ $p_2$ and really get PM = 45° (w/o worrying about the influence of $p_3$)

③ Eliminate $p_2$ by placing $z_1$ on top of it:

$$z_1 = p_2 \Rightarrow \frac{1}{C_c\left(\frac{1}{g_{mII}} - R_z\right)} = -\frac{g_{mII}}{C_{II}}$$

$$R_z = \frac{(C_c + C_{II})}{C_c}\left(\frac{1}{g_{mII}}\right) = \frac{1}{g_{mII}}\left(1 + \frac{C_{II}}{C_c}\right)$$




With this choice of $R_z$:

$$p_3 = -\frac{1}{R_z C_I} = -\frac{1}{\left(\frac{C_c + C_{II}}{C_c}\right)\left(\frac{1}{g_{mII}}\right) C_I}$$

$$p_3 = -\frac{g_{mII} C_c}{C_I (C_c + C_{II})}$$

This is the new $p_2$

For PM = 45°:

$$C_c = \frac{g_{mI}}{|p_3| A_0} = \frac{g_{mI}}{g_{mII}} \frac{C_I (C_c + C_{II})}{C_c A_0}$$

↳ the "new" $|p_2|$ ↘ solve for $C_c$

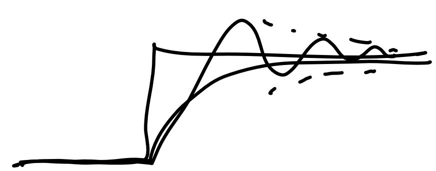
For PM = 60°:

$$C_c = \frac{1.73\, g_{mI}}{|p_3| A_0} \rightarrow C_c \cong \sqrt{1.73 \frac{g_{mI}}{g_{mII}} \frac{C_I C_{II}}{A_0}}$$

$[C_I \ll C_{II}]$ ↑ For PM = 60°

Remark. If settling time is important, then approach ③ may not be the best approach. The reason is that if the zero is not exactly equal to the pole, the a "doublet" ensues, which actually can hurt the settling time.

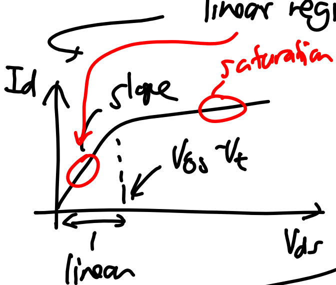
↑ Discussed in a handout to be posted on the course website. → also, discussed in Razavi, problem 10.19.



## Actual Implementation

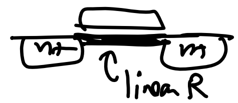
⇒ resistors are too big! → ∴ implement using a much smaller MOS resistor!

**MOS Resistor:** just an MOS Xsistor operated in the linear region




$$I_d = \mu_n C_{ox}\frac{W}{L}\left[(V_{gs}-V_t)V_{ds} - \frac{1}{2}V_{ds}^2\right]$$

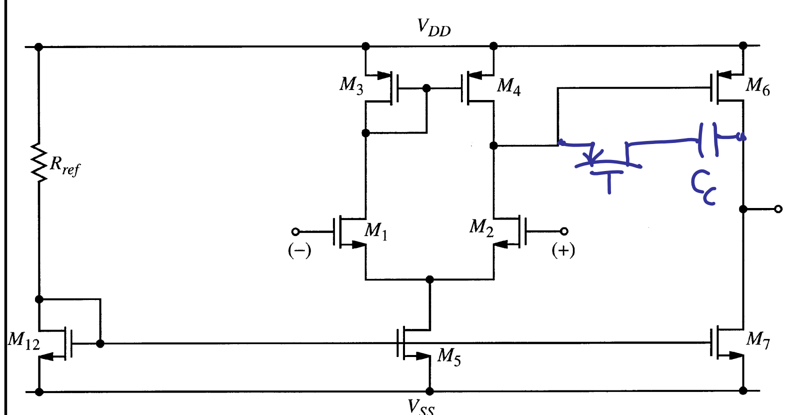
$$\frac{\partial I_d}{\partial V_{ds}} = \mu_n C_{ox}\frac{W}{L}(V_{gs}-V_t-V_{ds})$$




$$R_{s.s.} = \left[\frac{dI_d}{dV_{ds}}\right]^{-1}_{V_{gs}=V_{GS},\,V_{ds}=V_{DS}} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t-V_{DS})} = \frac{1}{g_{ds}}$$

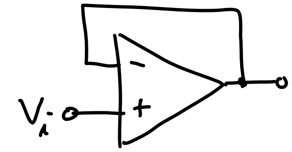
↑ a variable resistor controllable by $V_{GS}$!

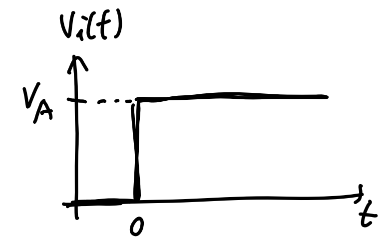
## Actual Implementation




(to be continued in the next lecture)

## Slew Rate (f/ before)




**Using Laplace Xform Theory:**

$$\frac{V_o}{V_i}(s) = \frac{1}{1+\frac{s}{\omega_1}} = \frac{1}{1+s\tau_1} \qquad \tau_1 = \frac{1}{\omega_1}$$

↖ single (dominant) pole

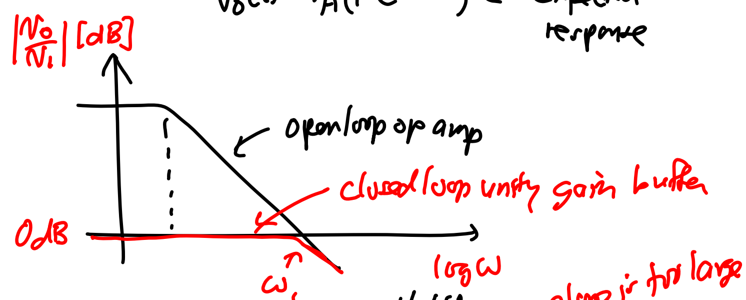
$$V_i(s) = \frac{V_A}{s}$$

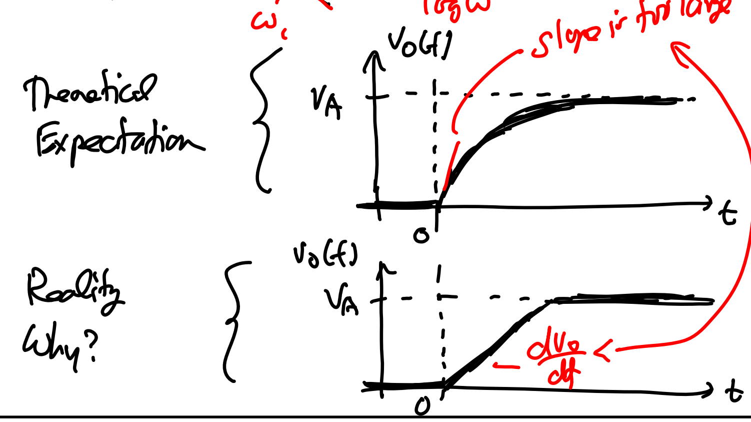
$$V_o(s) = \frac{V_A}{s(1+s\tau_1)} = \frac{V_A}{s} - \frac{V_A}{s+\frac{1}{\tau_1}}$$

⇕ Inverse Laplace Xform

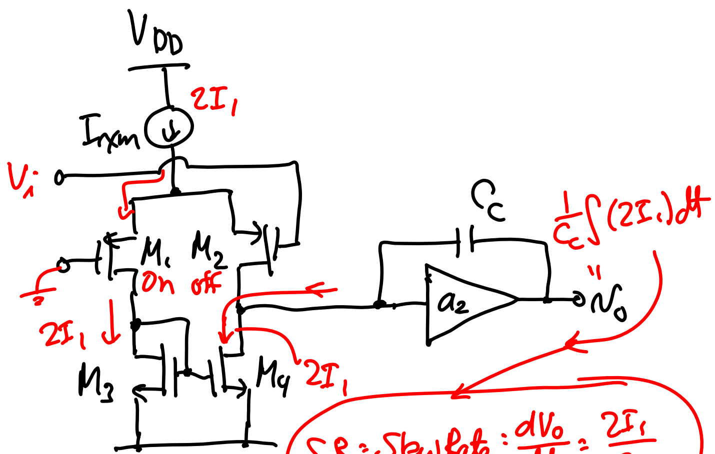
$$V_o(t) = V_A(1-e^{-t/\tau_1})$$

← expected response (the constant $\tau_1$)



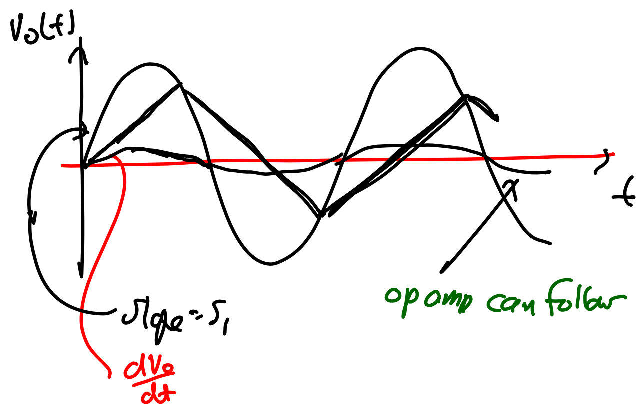



Reason: 1st & 2nd stage of op amp cannot source enough current to mimic the shape (or speed) of a fast rising input signal




$$S.R. = \text{Slew Rate} = \frac{dV_o}{dt} = \frac{2I_1}{C_C}$$

Ex. If apply a very fast (i.e., high freq., large amplitude) sinusoid:




In terms of design variables:

$$S.R. = \frac{dV_o}{dt} = \frac{I_{XM}}{C_C} = \boxed{\frac{I_{XM}}{G_{m1}}\omega_{ult}A_o = S.R.}$$

$$C_C = \frac{G_{m1}}{\omega_{ult}A_o} \leftarrow \text{closed-loop gain}$$

$\omega_{ult} = \omega @ |a(j\omega)f| = 1$

To Increase S.R.:

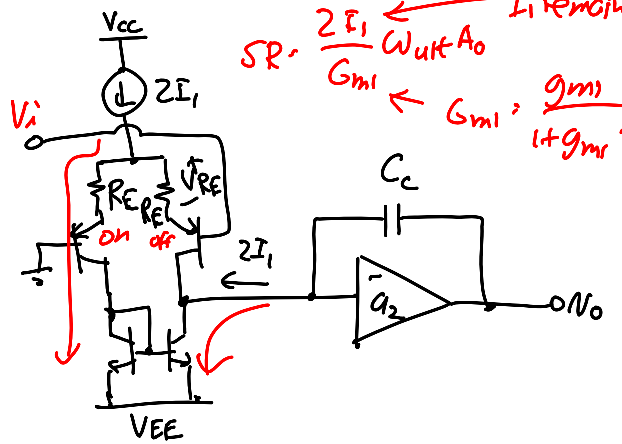
1. Decrease $G_{m1}$ ← transconductance of 1st stage
2. Increase $\omega_{ult}$ → increase $\omega_2$
   ↘ limited by the Xstr freq. range
3. Use a larger $A_o$, if possible.
   closed loop gain (only if permitted by the application)

## Increasing S.R. via $G_m$-Reduction

① Emitter or Source Degeneration of the Input Stage –

$SR = \frac{2I_1}{G_{m1}}\omega_{ult}A_o$ ← $I_1$ remains the same

$G_{m1} = \frac{g_{m1}}{1+g_{m1}R_E}$ ↓ → SR↑



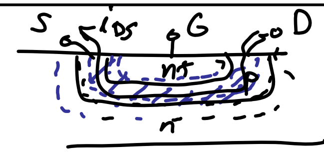

Limitations:

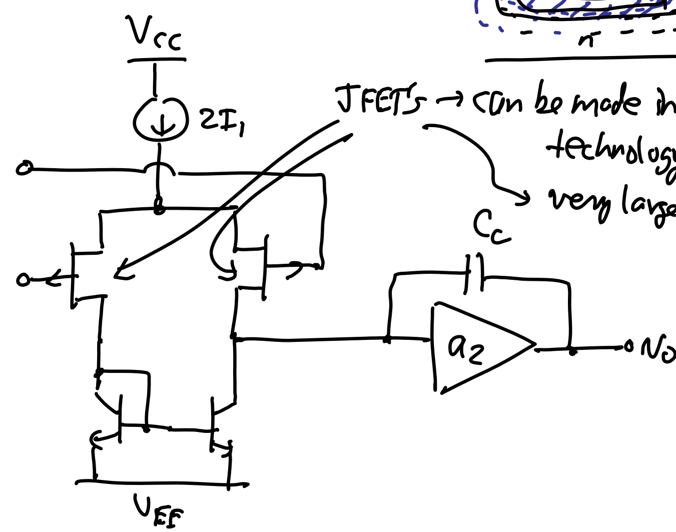
① $R_E$ mismatch → $V_{OS}$
↳ must limit $V_{RE}$ to limit $V_{OS}$

② $R_E$↑ → gain↓ (SR-gain trade-off)

③ $R_E$ contributes thermal noise → must limit to preserve the noise performance of the op amp.

② FET Input Devices –




JFETs → can be made in bipolar technology
↳ very large $R_i$

For FET's: $\frac{g_m}{I_D} \approx \frac{2}{V_{GS}-V_t}$ ← ~0.2V

For BJT's: $\frac{g_m}{I_C} = \frac{1}{V_T}$ ← 26 mV

$$\frac{\text{FET S.R.}}{\text{BJT S.R.}} = \frac{\frac{I_D}{g_{mF}}\omega_{ult}}{\frac{I_C}{g_{mB}}\omega_{ult}} = \frac{\frac{V_{GS}-V_t}{2}}{V_T} = \frac{V_{GS}-V_T}{2V_T} = \frac{260}{26} \approx 10$$

Limitations:

① Higher $V_{OS}$.

② Increased voltage noise.
(But decreased current noise.)

## Settling Time

response to a step $V_i$:

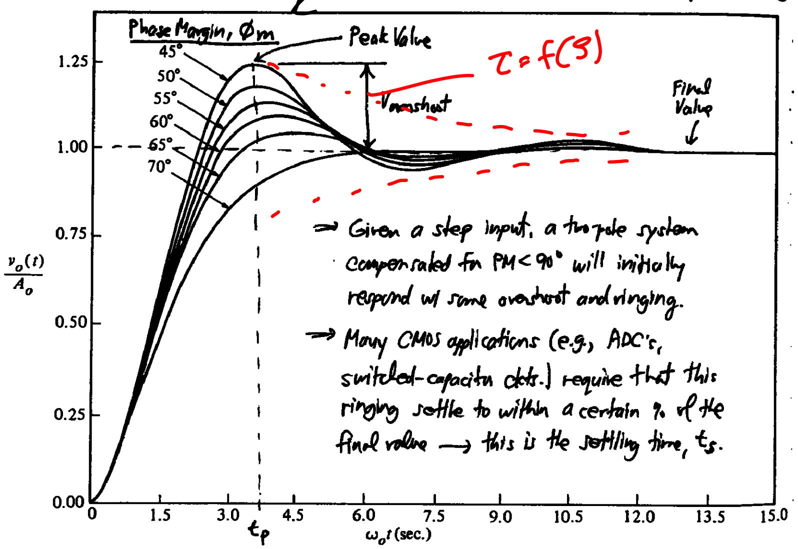



**Figure 8.2-3** Response of second-order system with various phase margins.

Obtain Expressions for:

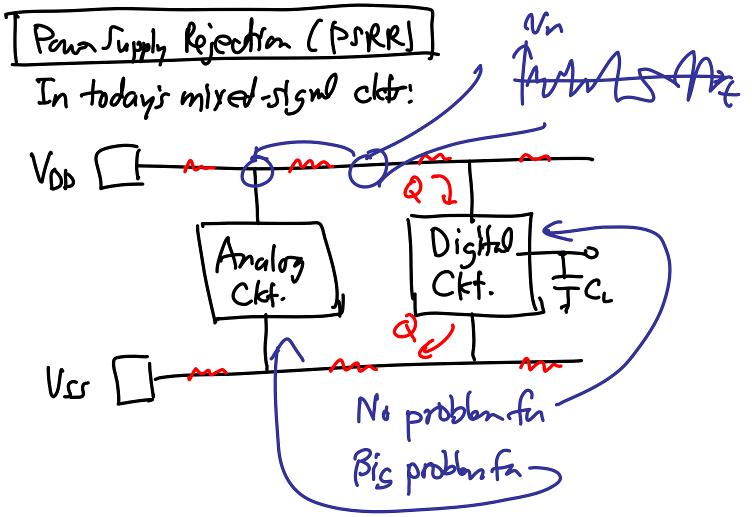
① $V_{overshoot}$
② Settling Time, $T_s$

} as functions of phase margin, $\phi_m$

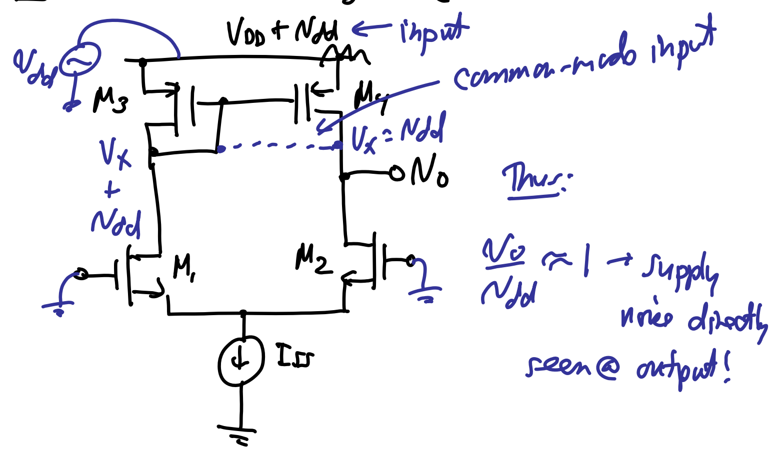
- Go through settling time handout

## Power Supply Rejection (PSRR)

In today's mixed-signal ckts:




Ex. CMOS Diff. Input Stage w/ Current Mirror Load




Thus: $\frac{v_o}{v_{dd}} \approx 1$ → supply noise directly seen @ output!

**Definition.** Power Supply Rejection Ratio (PSRR)

$$PSRR \triangleq \frac{\text{Gain From Input to Output}}{\text{Gain From Supply to Output}} = \frac{A_v|_{v_{dd}=0}}{A_{dd}|_{v_i=0}}$$

Thus, for the above example:

$$PSRR \cong \frac{g_{m2}(r_{o2} \| r_{o4})}{1} \rightarrow \boxed{PSRR \cong g_{m2}(r_{o2} \| r_{o4})}$$

For more complicated circuits, much more work is involved.

↳ to make things easier, use a unity gain configuration

Can also get PSRR = f(ω)