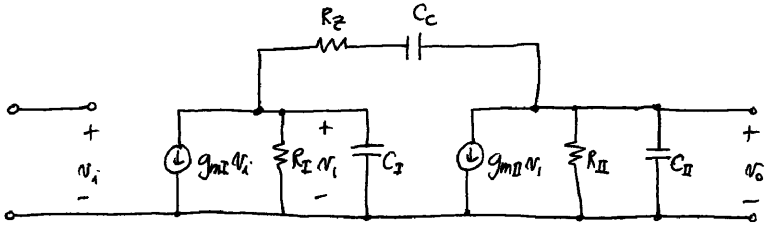
Lecture 25: Feedback Configurations

- Announcements:
- Design Project Checkpoint:
  - Due Monday, April 23, 11:59 p.m.
  - Send to your TA a spice file for your op amp design that simulates correctly, i.e., that reaches a stable bias point where all transistors are saturated (or linear if an MOS resistor)
  - It doesn't need to meet the project specs, but it should simulate correctly
- Lecture Topics:
  - Nulling the RHP Zero (revisit w/ practical implementation)
  - Power Supply Rejection Ratio (PSRR) – finish w/ an example
  - Advantages of Feedback (revisited)
  - Feedback Configurations
  - Effect of FB on Z_i and Z_o
- ----------
- Last Time:

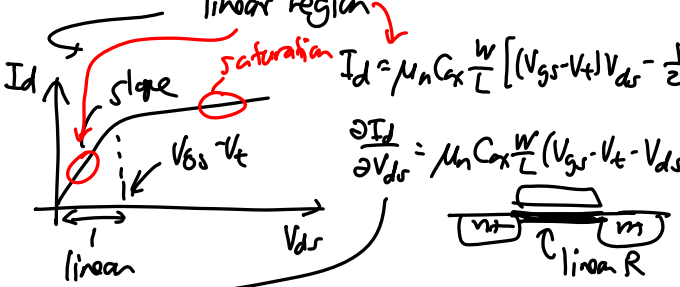
Nulling Resistor in Series w/ C_C



Actual Implementation

⇒ resistor are too big! → ∴ implement using a much smaller MOS resistor!

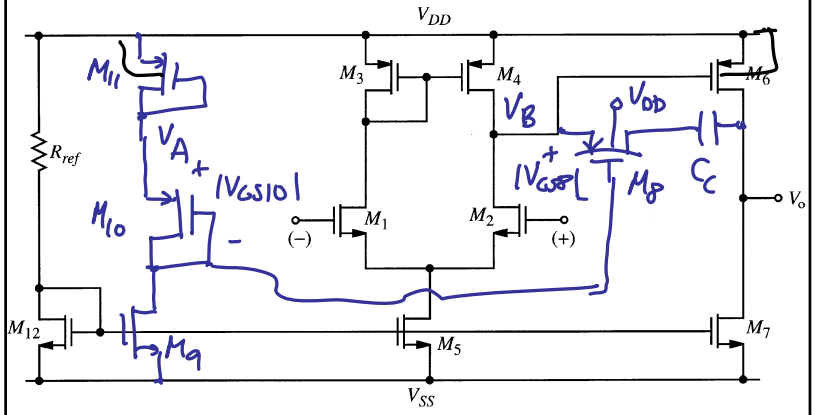
MOS Resistor: just an MOS transistor operated in the linear region



$$R_{s.s.} = \left[\frac{dI_d}{dV_{ds}}\right]^{-1}_{V_{gs}=V_{GS},V_{ds}=V_{DS}} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t-V_{DS})} = \frac{1}{g_{ds}}$$

a variable resistor controllable by V_{GS}!

Actual Implementation



Design

Need $V_A = V_B \rightarrow |V_{GS11}| = |V_{GS6}|$, know that $|V_{t11}| = |V_{t6}|$

$$\sqrt{\frac{2I_{D11}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{11}}} = \sqrt{\frac{2I_{D6}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_6}}$$

$$\left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_6 \frac{I_{D11}}{I_{D6}} = \left(\frac{W}{L}\right)_6 \frac{I_{D10}}{I_{D6}}$$

Also, need $|V_{GS10}| = |V_{GS8}|$

Because $V_A = V_B \rightarrow V_{S10} = V_{S8} \rightarrow |V_{t10}| = |V_{t8}|$

$$\therefore |V_{ov10}| = |V_{ov8}| = \sqrt{\frac{2I_{D10}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{10}}}$$

Thus:

$$R_8 = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_8 \sqrt{\frac{2I_{D10}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{10}}}} = \frac{\sqrt{\mu_p C_{ox}(W/L)_{10}}}{\mu_p C_{ox}(W/L)_8 \sqrt{2I_{D10}}}$$

Case: Eliminate p_2 by placing z_1 on top of it.

$$R_2 = \frac{C_c + C_L}{g_{m6} C_c} = \frac{\sqrt{\mu_p C_{ox}(W/L)_{10}}}{\mu_p C_{ox}(W/L)_8 \sqrt{2I_{D10}}}$$

$$\sqrt{2\mu_p C_{ox}(W/L)_6 I_{D6}}$$

$$\left(\frac{W}{L}\right)_8 = \sqrt{\left(\frac{W}{L}\right)_6 \left(\frac{W}{L}\right)_{10} \frac{I_{D6}}{I_{D10}} \cdot \left(\frac{C_c}{C_c + C_L}\right)}$$

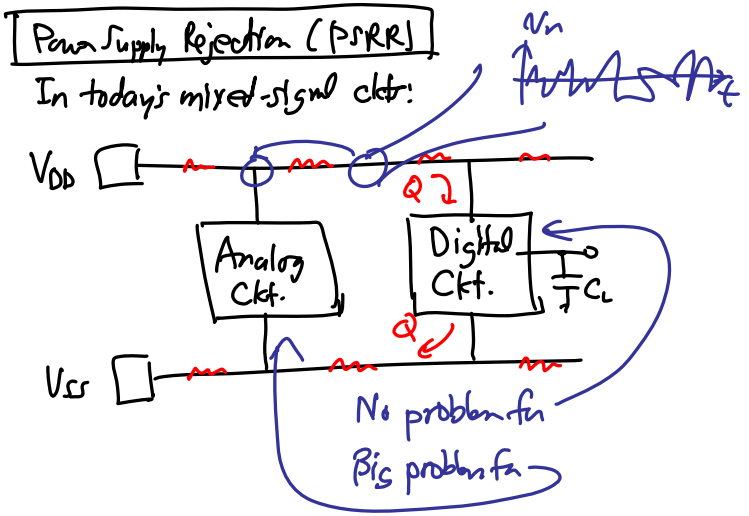
Case: Move $z_1 \rightarrow \infty$.

$$R_2 = \frac{1}{g_{m6}} \Rightarrow \left(\frac{W}{L}\right)_8 = \sqrt{\left(\frac{W}{L}\right)_6 \left(\frac{W}{L}\right)_{10} \frac{I_{D6}}{I_{D10}}}$$

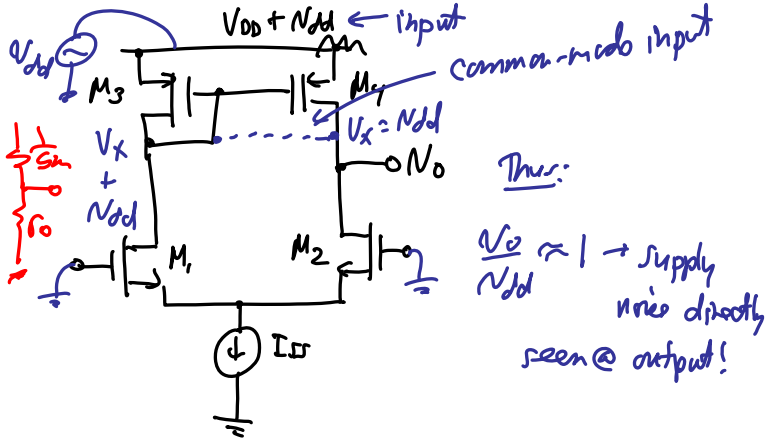
over

Power Supply Rejection (PSRR)

In today's mixed-signal ckts:



Ex. CMOS Diff. Input Stage w/ Current Mirror Load



Definition. Power Supply Rejection Ratio (PSRR)

$$PSRR \triangleq \frac{\text{Gain From Input to Output}}{\text{Gain From Supply to Output}} = \frac{A_N|_{N_{dd}=0}}{A_{dd}|_{N_i=0}}$$

Thus, for the above example:

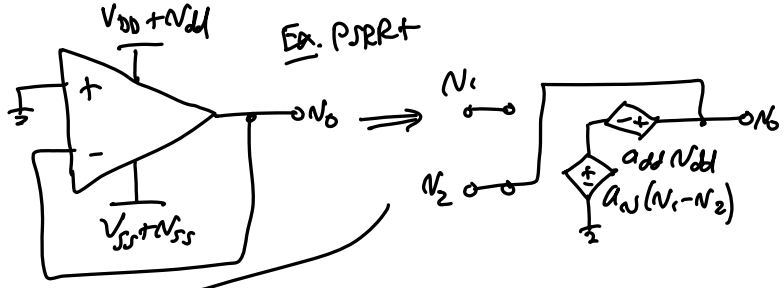
$$PSRR \cong \frac{g_{m2}(r_{o2}\|r_{o4})}{1} \Rightarrow \boxed{PSRR \cong g_{m2}(r_{o2}\|r_{o4})}$$

For more complicated circuits, much more work is involved.

↳ to make things easier, use a unity gain configuration

Can also get PSRR = f(ω) $a_{dd} = \frac{N_o}{N_{dd}}$

Ex. PSRR+



$$N_o = a_N(N_i - N_2) + a_{dd}N_{dd}$$

$$= -N_o$$

$$N_o(1 + a_N) = a_{dd}N_{dd}$$

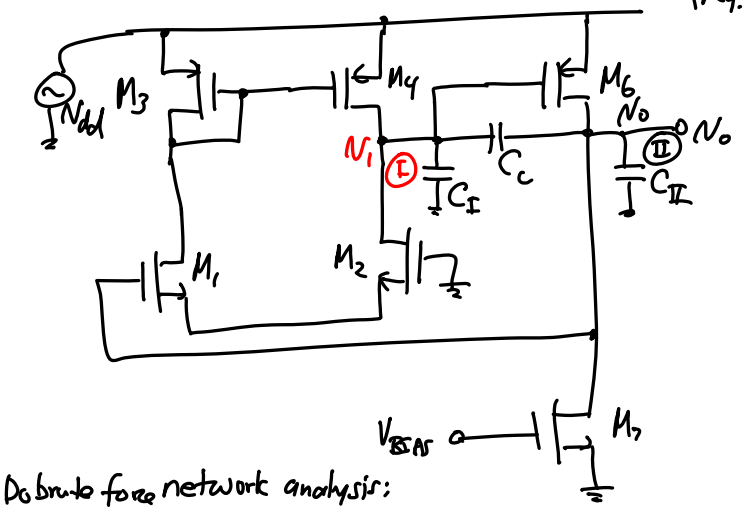
$$\frac{N_o}{N_{dd}} = \frac{a_{dd}}{1+a_N} = \frac{1}{\frac{1}{a_{dd}} + \frac{a_N}{a_{dd}}} \cong \boxed{\frac{1}{PSRR+} = \frac{N_o}{N_{dd}}}$$

Just find this Xfer fcn to get PSRR+ when the op amp is hooked into unity gain FB

$$\boxed{PSRR+ = \frac{N_{dd}}{N_o}}$$

Two-Stage Op Amp PSRR+

Want PSRR+ = f(ω) (ω ↑ freq.)



Do brute force network analysis:

KCL (I): $G_I V_{dd} = (G_I + sC_c + sC_I) V_1 - (g_{mI} + sC_c) V_o$

KCL (II): $(g_{mII} + g_{ds6}) V_{dd} = (g_{mII} - sC_c) V_1 + (G_{II} + sC_c + sC_{II}) V_o$

$G_I = g_{ds1} + g_{ds4} = g_{ds2} + g_{ds4}$

$G_{II} = g_{ds6} + g_{ds7}$

$g_{mI} = g_{m1} = g_{m2}$

$g_{mII} = g_{m6}$

$[g_{ds} = \frac{1}{r_o}]$ ← For saturated device.

math & rearranging

Get:

$$\left.\frac{V_{dd}}{V_o}\right|_{closed\text{-}loop} = \frac{N(s)}{D(s)} = \frac{(\quad)}{(\quad)} \quad \text{polynomials}$$

↳ then use: $N(s) = 1 + \left(\frac{s}{z_1} + \frac{s}{z_2}\right) + \frac{s^2}{z_1 z_2} \approx 1 + \frac{s}{z_1} + \frac{s^2}{z_1 z_2}$

$$PSRR+ = A_{vo}^{+} \left[\frac{\left(1 + \frac{s}{GB}\right)\left(1 + \frac{s}{|p_2|}\right)}{\left(1 + \frac{s}{GB/A_{vo}^{+}}\right)}\right]$$

where GB = Gain BW product = $\frac{g_{mI}}{C_c}$

A_{vo}^{+} = DC PSRR+ = $\frac{g_{mI} g_{mII}}{G_I g_{ds6}}$

$|p_2| = \frac{g_{mII}}{C_{II}}$ $\omega_p^{+} = \frac{GB}{A_{vo}^{+}}$

To maximize PSRR+: (@dc) decrease g_{ds6}, raise g_{mII}

$$PSRR^{-} = A_{vo}^{-} \left[\frac{\left(1 + \frac{s}{GB}\right)\left(1 + \frac{s}{|p_2|}\right)}{\left(1 + \frac{s}{\omega_p^{-}}\right)}\right]$$

where $A_{vo}^{-} = \frac{g_{mI} g_{mII}}{G_I g_{ds7}}$

$GB = \frac{g_{mI}}{C_c}$ $\omega_p^{-} = \frac{G_I}{C_c + C_I} \approx \frac{G_I}{C_c}$

$|p_2| = \frac{g_{mII}}{C_{II}}$

To maximize PSRR−: ① decrease g_{ds7}

② increase $g_{mII} = g_{m6}$

Remarks.

① Since often $g_{ds7} < g_{ds6}$ → often PSRR⁻ > PSRR⁺ (@dc)

② $$\frac{\omega_p^-}{\omega_p^+} = \frac{\cancel{g_{m1}}/\cancel{C_c}}{\cancel{C_1} g_{ds6} / g_{m2}\cancel{C_c}} = \frac{g_{m2}}{g_{ds6}}$$ → that's quite large

$\therefore \omega_p^- \gg \omega_p^+$

Thus, for an NMOS input op amp, PSRR⁻ is often better than PSRR⁺. → in design, need to worry more about PSRR⁺!

③ Some methods for reducing PSRR:

(i) Use buffer-based zero-cancellation in the compensation loop.

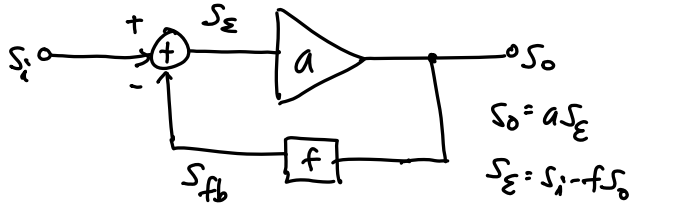
(ii) Use cascode circuitry, or balanced circuit topologies.

(iii) Supply-independent biasing.

(iv) Design strategies to minimize parasitic capacitive feedthrough.

Feedback

⇒ we know this:



$S_o = a S_\varepsilon$

$S_\varepsilon = S_i - f S_o$

$$\Rightarrow \boxed{\frac{S_o}{S_i} = \frac{a}{1+af} = A}$$

Benefits of Negative FB

① Stabilizes the gain of the amp against parameter changes & active device variations

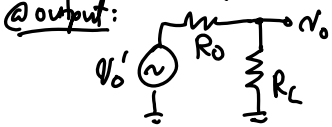
② Modifies R_i and R_o → basically improves their values according to the type of amplifier implemented

e.g., voltage amp: R_i: large, R_o: small

@ input:

If R_i: large, $V_i \approx V_s$. ($R_i \gg R_s$)

@ output:



If R_o: small, $V_o \approx V_o'$. ($R_o \ll R_L$)

current-to-voltage amp: R_i: small, R_o: small

voltage-to-current amp: R_i: large, R_o: large

current-to-current amp: R_i: small, R_o: large

③ Reduces distortion; improves linearity.

④ Increases bandwidth (ω_{-3dB}).

Disadvantages of Neg. FB

① Gain is reduced → reduction factor ~ equal to the amount of gain stabilization, distortion reduction, etc...

Solution: Add more stages of gain → but this adds cost & power...

② Feedback causes stability problems (if not compensated properly)

Gain Sensitivity Reduction Via FB

$$A = \frac{a}{1+af} \rightarrow \frac{dA}{da} = \frac{(1+af) - af}{(1+af)^2} = \frac{1}{(1+af)^2}$$

For a Δ in op amp gain: δa

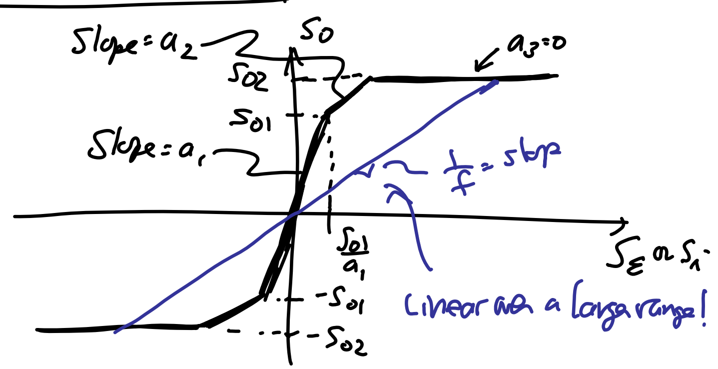
$$\frac{\delta A}{\delta a} = \frac{1}{(1+af)^2} \longrightarrow \delta A = \frac{\delta a}{(1+af)^2}$$

↑ much smaller than δa

... and the fractional change:

$$\frac{\delta A}{A} = \frac{1+af}{a}\,\frac{\delta a}{(1+af)^2} \Rightarrow \boxed{\frac{\delta A}{A} = \frac{\frac{\delta a}{a}}{1+af}}$$

Distortion Reduction via FB



Now, close the loop:

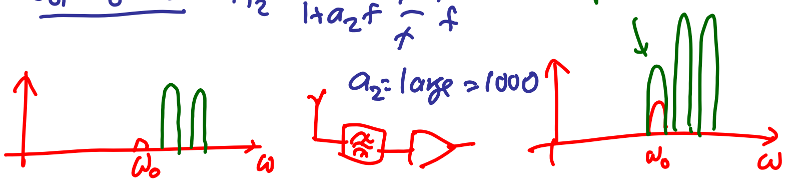
for a_1: large ≈ 20K

$0 < S_o < S_{o1}$: $A_1 = \frac{a_1}{1+a_1 f} \approx \frac{1}{f}$

$S_{o1} < S_o < S_{o2}$: $A_2 = \frac{a_2}{1+a_2 f} \approx \frac{1}{f}$

a_2: large ≈ 1000

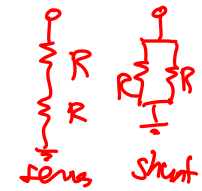
distortion (nonlinearity) → masks the w_o signal



"Inspection" Analysis of FB Ckts.

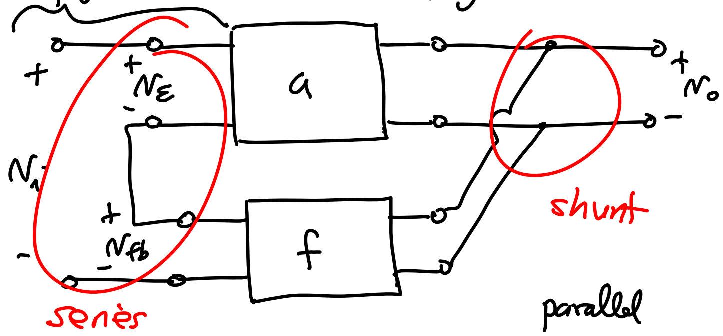
↓ start with...

Identification of FB Connection Types



Series Connection – FB network port in series w/ amplifier port

↳ must go thru both the FB port & the amplifier port to get from the node of interest to ground



parallel

Shunt Connection – FB network port in shunt w/ amplifier port

↳ can get from the node of interest to ground via either FB network port or the amplifier port

Given: