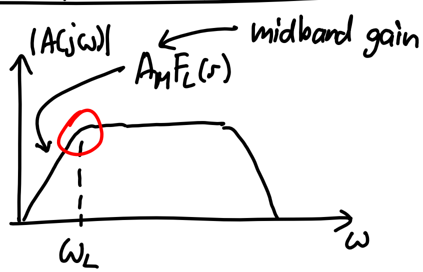
Lecture 7: Frequency Response Inspection Analysis II

- **Announcements**:
- This is our make-up lecture for next Tuesday
- No lecture next Tuesday, but there will be lecture next Thursday
- **Lecture Topics**:
  - Frequency Response Examples (cont.)
  - Short Ckt Time Constant (SCTC) Analysis
  - Example Low Freq. Response Determination
  - Start Active Loads
- -----------------------------------
- **Last Time**:

$\boxed{\text{Low Freq. Amplifier Response Using Short Circuit Time Constant Analysis (SCTC)}}$

Recall:



In general, for the low freq. response:

$$F_L(s) = \frac{s^{n_L} + d_1 s^{(n_L-1)} + \cdots}{s^{n_L} + e_1 s^{(n_L-1)} + \cdots}, \quad n_L = \#\text{poles} = \#\text{zeros}$$

We can express the coefficient e_1 by:

$$e_1 = \omega_{P1} + \omega_{P2} + \cdots + \omega_{Pn_L}$$

Similar analysis to that used for OCTC...

For the case of a dominant pole:
↳ i.e., the highest freq. pole

$$F_L(s) \cong \frac{s}{s+\omega_L} = \frac{s}{s+e_1} \rightarrow e_1 \cong \omega_{P1} = \omega_L$$

$$\therefore \boxed{\omega_L \cong e_1 = \sum_j \omega_{Pj} = \sum_j \frac{1}{C_j R_{js}} = \sum_j \frac{1}{\tau_{js}}}$$

where $C_j \triangleq$ various large (>10nF) capacitors in the ckt. (e.g., the bypass caps.)

$R_{js} \triangleq$ driving point resistance seen between the terminals of C_j determined with:

For reading, can go to Sedra & Smith

① all large capacitors short-circuited, except C_j, which is replaced by the test voltage source for R determination

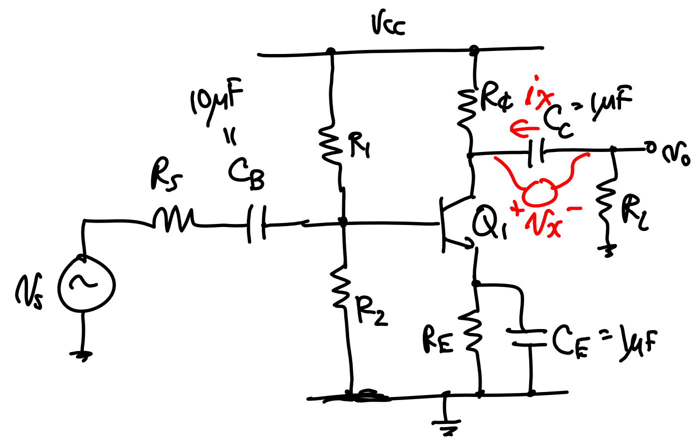
② all independent sources eliminated (i.e., short voltage sources, open current sources)

③ open all H.F. capacitors (i.e., small caps in the pF range, or <1nF)

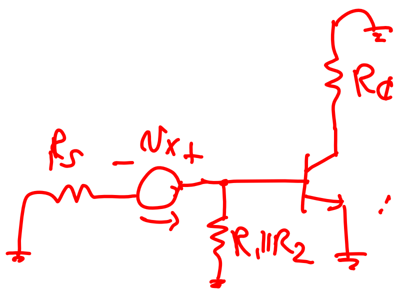
Again, for the case where there are no dominant poles, a reasonable approximation is:

$$\omega_L \cong \sqrt{\omega_{P1}^2 + \omega_{P2}^2 - 2\omega_{Z1}^2 - 2\omega_{Z2}^2}$$

Ex. Determine the L.F. Response of the C.E. Amplifier



(a) Find τ due to C_B: short ckt. C_c & C_E



$R_{Bs} = \frac{v_x}{i_x}$ = resistance in series w/ v_x

$\therefore R_{Bs} = R_s + r_\pi || R_1 || R_2$

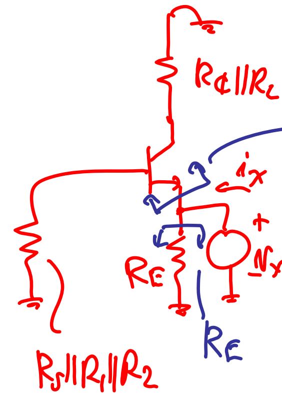
$\tau_B = R_{Bs} C_B = (R_s + r_\pi || R_1 || R_2) C_B$

$$\omega_{pB} = \frac{1}{\tau_B} = \frac{1}{(R_s + r_\pi || R_1 || R_2) C_B}$$

(b) τ due to C_c: short ckt. C_B & C_E
→ again, it will be R in series

$$\tau_c = (R_L + \underbrace{r_o || R_C}_{\approx R_C}) C_c \rightarrow \omega_{pc} = \frac{1}{\tau_c} = \frac{1}{(R_L + R_C) C_c}$$

(c) τ due to C_E: short C_B & C_c



$$\frac{r_\pi + R_s || R_1 || R_2}{\beta + 1}$$

$$R_{Es} = R_E \,\Big|\Big|\, \frac{r_\pi + R_s || R_1 || R_2}{\beta + 1}$$

$\tau_E = R_{Es} C_E$

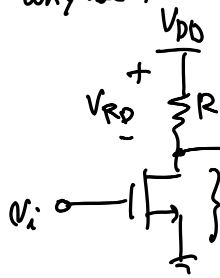
$$\omega_{pE} = \frac{1}{\tau_E} = \frac{1}{R_{Es} C_E}$$

And finally:

$$\omega_L = \omega_{pB} + \omega_{pc} + \omega_{pE}$$

Active Loads

⇒ Why use them? → Gain: $\frac{v_o}{v_i} = -g_m R_D$



For $\frac{v_o}{v_i}$ ↑, must:

① Raise g_m → raise I_D

→ Problem: V_{R_D} ↑

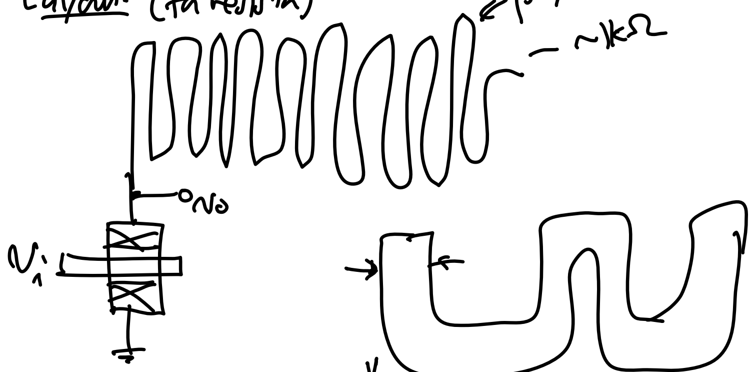
→ V_{ov} → V_{DS} ↓

→ MOS saturated → linear → lose gain!

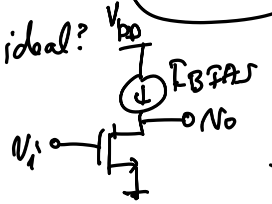
② increase R_D → same problem

↘ also, area!

Layout: (for resistor)



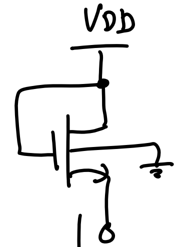
⇒ what would be ideal?



} to set this & use active load!

Types of Active Loads → want a current source

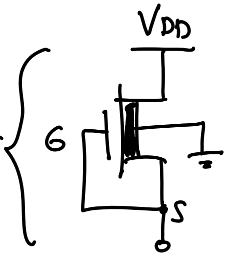
Diode-Connected Enhancement Load:



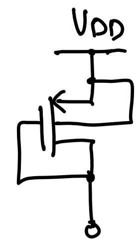
to drive Xsistor

Depletion Load:

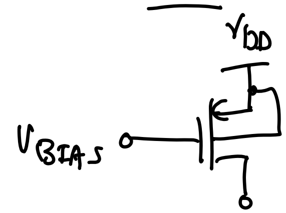
ancient & we won't consider this



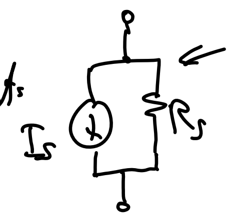
Diode-Connected PMOS Load:



PMOS Current Source Load:

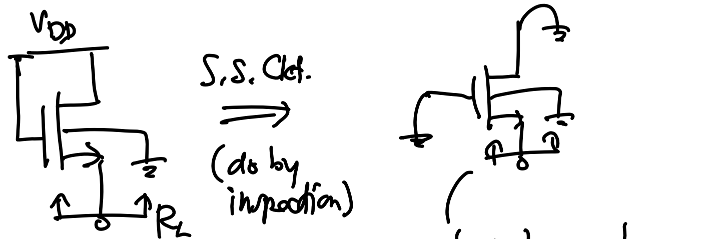


Norton Equivalent:



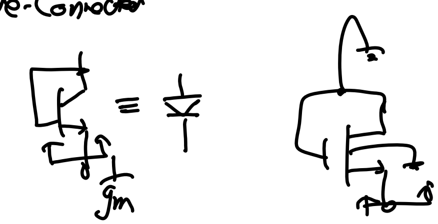
← ideal when $R_S = \infty$

Diode-Connected Enhancement Load

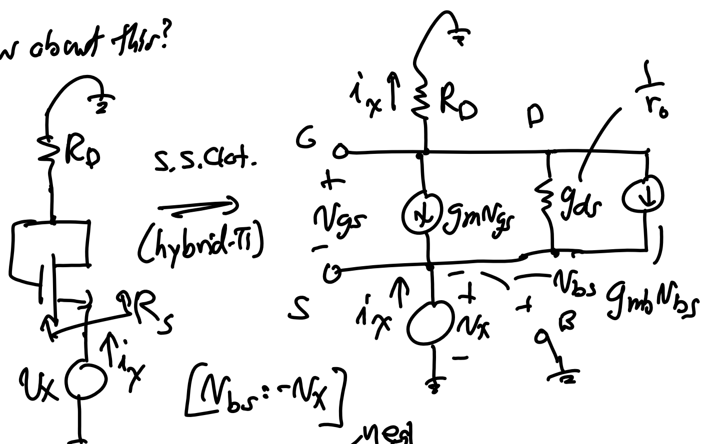


$$R_L = \frac{1}{g_m} \,\|\, \frac{1}{g_{mb}} = \frac{1}{g_m + g_{mb}} \sim 1\text{-}10k\Omega$$

"Diode-Connected"



How about this?



$[v_{bs} = -v_x]$

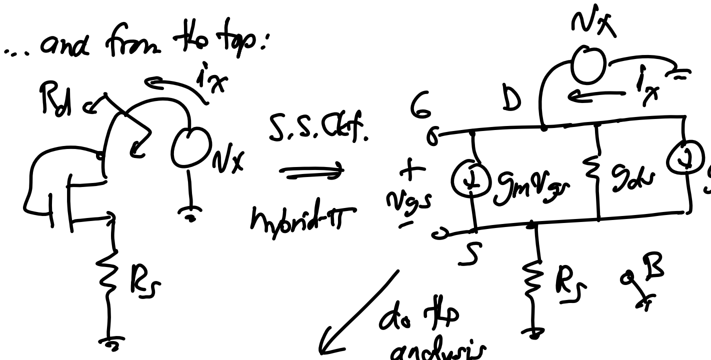
negl.

$$i_x = -g_m v_{gs} + \cancel{g_{ds}(-v_{gs})} - g_{mb} v_{bs}$$
$$= g_m(v_x - i_x R_D) + g_{mb} v_x$$

$$R_S = \frac{v_x}{i_x} = \frac{1 + g_m R_D}{g_m + g_{mb}} = \frac{1}{g_m + g_{mb}} + \frac{R_D}{1+\eta}$$
$$\approx \frac{1}{g_m + g_{mb}} + R_D$$

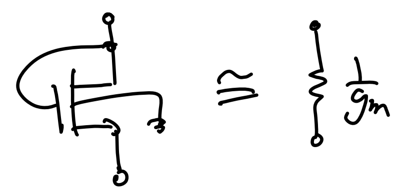
$$\boxed{R_S \cong \frac{\frac{1}{g_m} + R_D}{1+\eta}}$$

... and from the top:

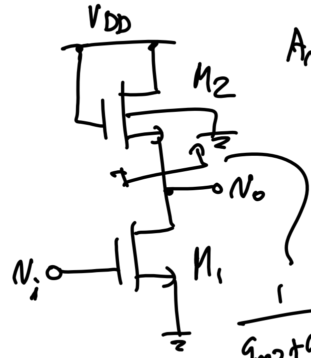


$$R_d = \frac{v_x}{i_x} = \frac{1}{g_m} + (1+\eta) R_S \approx \frac{1}{g_m} + R_S$$

Thus:



Apply to a C.S. Ckt.

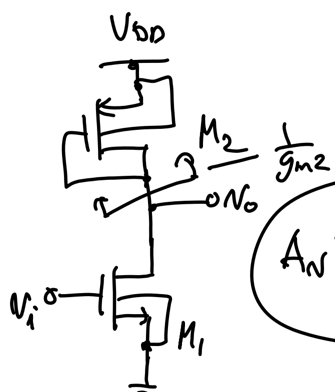


$\frac{1}{g_{m2}+g_{mb2}}$

$$A_v = \frac{v_o}{v_i} = -\frac{g_{m1}}{g_{m2}+g_{mb2}} = -\frac{1}{(1+\eta)}\frac{g_{m1}}{g_{m2}} = A_v$$

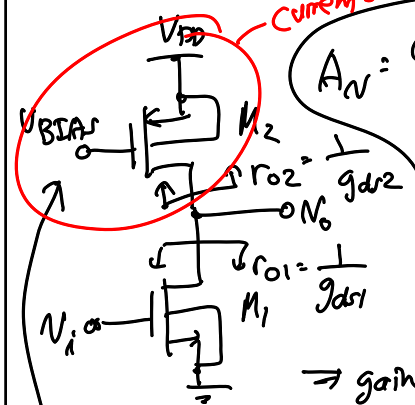
$$A_v = -\frac{1}{1+\eta}\frac{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_1 I_D}}{\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_2 I_D}} = -\frac{1}{1+\eta}\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

Diode-Connected PMOS Load



$$A_v = -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{\mu_n (W/L)_1}{\mu_p (W/L)_2}}$$

PMOS Current Source Load

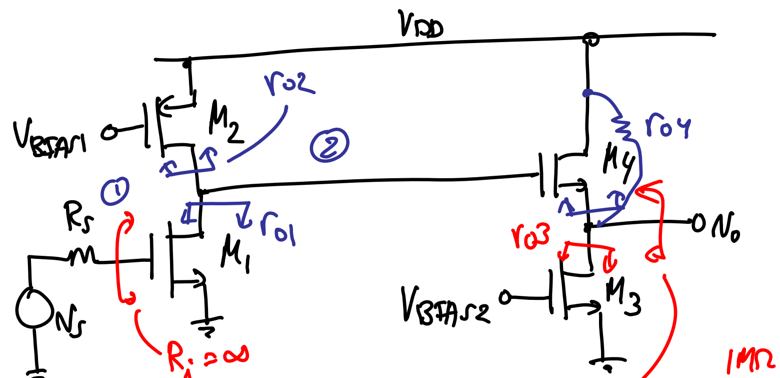


$$A_v = \frac{v_o}{v_i} = -g_{m1}(r_{o1} \| r_{o2}) = -\frac{g_{m1}}{g_{ds1}+g_{ds2}}$$

⇒ gain is huge! (r_o: huge ~1MΩ)

⇒ but requires V_{BIAS}!

Ex. Multistage Actively Loaded MOS Ckt.



Want R_i, R_o, A_v, ω_H.

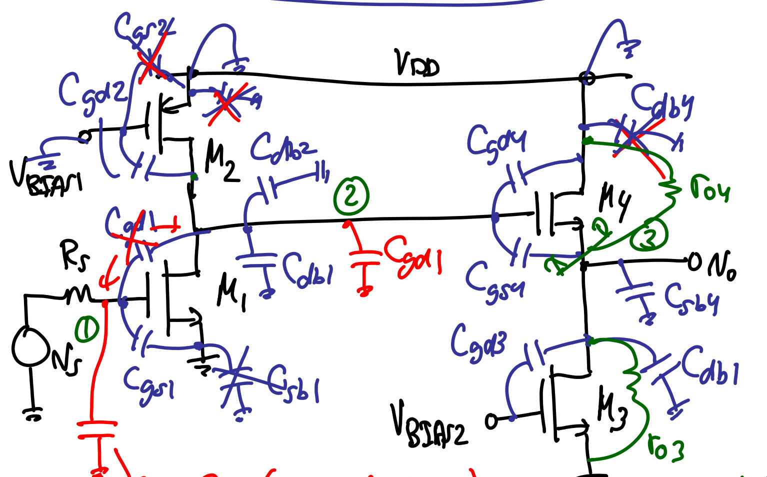
$$R_o = \frac{1}{g_{m4}+g_{mb4}} \| r_{o3} \approx \frac{1}{g_{m4}+g_{mb4}}$$

kΩ, 1MΩ

$$a_v = \frac{v_{1}}{v_s}\cdot\frac{v_{2}}{v_{1}}\cdot\frac{v_o}{v_{2}}$$

$$= (1)\left(-g_{m1}(r_{o2}\|r_{o1})\right)\frac{g_{m4}(\cancel{r_{o3}\|r_{o4}})}{\cancel{1+}(g_{m4}+g_{mb4})(\cancel{r_{o3}\|r_{o4}})}$$

$$\therefore a_v = -g_{m1}(r_{o1}\|r_{o2})\left[\frac{g_{m4}}{g_{m4}+g_{mb4}}\right]$$



$C_M = C_{gd1}(1+\underbrace{g_{m1}(r_{o1}\|r_{o2})}_{\text{big!}})$ big! $\therefore$

These dominate!

huge!

$$\tau_1 = \left[C_{gs1}+C_{gd1}(1+g_{m1}(r_{o1}\|r_{o2}))\right]R_s$$

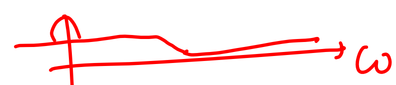
$$\tau_2 = (C_{gd1}+C_{db1}+C_{gd2}+C_{db2}+C_{gd4})(r_{o1}\|r_{o2})$$

$$\tau_3 = (C_{db3}+C_{gd3}+C_{sb4})\left[\frac{1}{g_{m4}+g_{mb4}}\right]$$

$$\tau_{gs4} = C_{gs4}\underbrace{\left[\frac{(r_{o1}\|r_{o2})+(r_{o3}\|r_{o4})}{\cancel{1+}(g_{m4}+g_{mb4})(r_{o3}\|r_{o4})}\right]}_{\frac{2}{g_{m4}+g_{mb4}}} \quad \times$$

from inspection formula ↓

but → there's a zero, too, in MOS



$$\boxed{\omega_H = \frac{1}{\tau_1+\tau_2+\cancel{\tau_3}+\cancel{\tau_{gs4}}}}$$