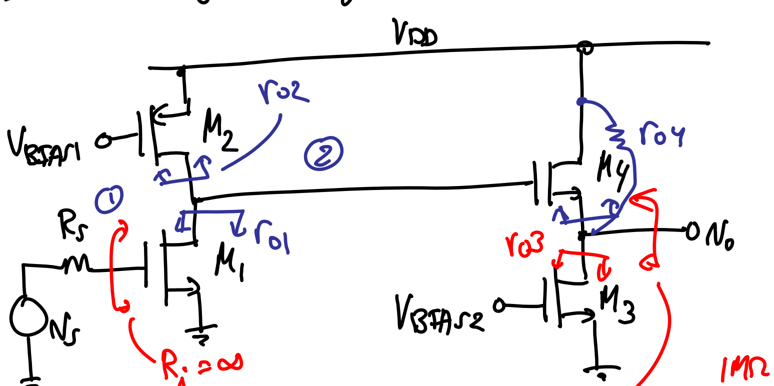
Lecture 8: Active Loads

- **Announcements:**
  - No Prof. Nguyen Office Hours on Monday or Thursday next week (on travel)
  - There WILL BE lecture Tuesday, next week
  - But NO LECTURE Thursday, next week???
  - Make-up lecture will probably be Friday in a room and time TBA
- **Lecture Topics:**
  - Analysis of actively loaded circuits (continued)
  - Current Sources
- ------------------------------------
- **Last Time:**

Ex. Multistage Actively loaded MOS Ckt.



Want R_i, R_o, A_v, ω_H.

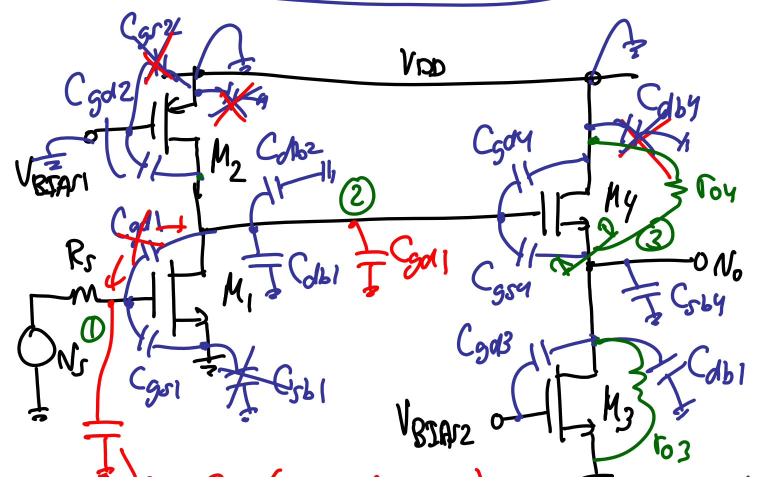
$$R_o = \frac{1}{g_{m4}+g_{mb4}} \| r_{o3} \approx \frac{1}{g_{m4}+g_{mb4}}$$

kΩ 1MΩ

$$a_v = \frac{v_{①}}{v_s}\cdot\frac{v_{②}}{v_{①}}\cdot\frac{v_o}{v_{②}}$$

$$= (1)(-g_{m1}(r_{o2}\|r_{o1}))\frac{g_{m4}(\cancel{r_{o3}\|r_{o4}})}{\cancel{1+}(g_{m4}+g_{mb4})(\cancel{r_{o3}\|r_{o4}})}$$

$$\boxed{\therefore a_v = -g_{m1}(r_{o1}\|r_{o2})\left[\frac{g_{m4}}{g_{m4}+g_{mb4}}\right]}$$



$C_M = C_{gd1}(1+\underline{g_{m1}(r_{o1}\|r_{o2})})$ big! ∴ big!

These dominate!

$$\tau_{①} = [C_{gs1} + C_{gd1}(1+g_{m1}(r_{o1}\|r_{o2}))]R_s \quad \text{huge!}$$

$$\tau_{②} = (C_{gd1} + C_{db1} + C_{gd2} + C_{db2} + C_{gd4})(r_{o1}\|r_{o2})$$

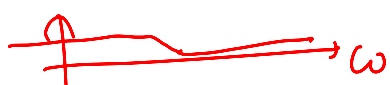
$$\tau_{③} = (C_{db3} + C_{gd3} + C_{sb4})\left[\frac{1}{g_{m4}+g_{mb4}}\right]$$

$$\tau_{gs4} = C_{gs4}\left[\frac{(r_{o1}\|r_{o2}) + (r_{o3}\|r_{o4})}{\underbrace{\cancel{1+}(g_{m4}+g_{mb4})(r_{o3}\|r_{o4})}_{\frac{2}{g_{m4}+g_{mb4}}}}\right] \quad X$$

from inspection formula

↓

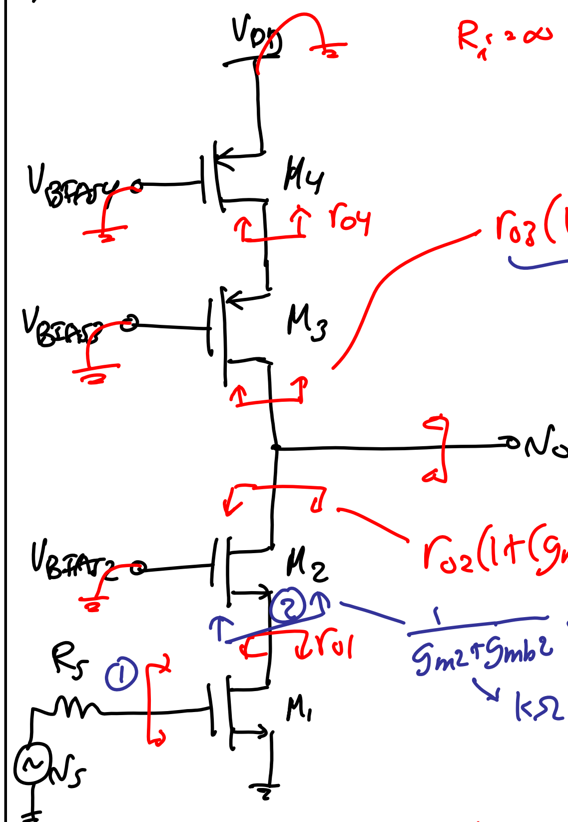
but → there's a zero, too, in MOS



$$\omega_H = \frac{1}{\tau_① + \tau_② + \cancel{\tau_③} + \cancel{\tau_{gs4}}}$$

Ex. Cascode Drive & Load

$R_i = \infty$



$$\underbrace{r_{o3}(1+(g_{m3}+g_{mb3})r_{o4})}_{r_{op}}$$

$$r_{o2}(1+(g_{m2}+g_{mb2})r_{o1})$$

$$\underbrace{\frac{1}{g_{m2}+g_{mb2}}}_{\to\ k\Omega} + \cancel{\frac{r_{op}}{r_{o2}\,g_{m2}}}$$

This actually could be significant, but let's ignore for now

$$R_o = \underbrace{\underbrace{r_{o2}(1+(g_{m2}+g_{mb2})r_{o1})}_{\sim g_{m2}r_{o1}r_{o2}} \,\|\, \underbrace{r_{o3}(1+(g_{m3}+g_{mb3})r_{o4})}_{\sim g_{m3}r_{o3}r_{o4}}}_{\sim \frac{g_m r_o^2}{2}} \Big\}\ \text{huge!}$$

$r_o \approx \frac{1}{\lambda I_D}$ ↘ $500k\Omega \to 1M\Omega$ ↘ $100M\Omega$

$g_m r_o \sim 100$

Get gain

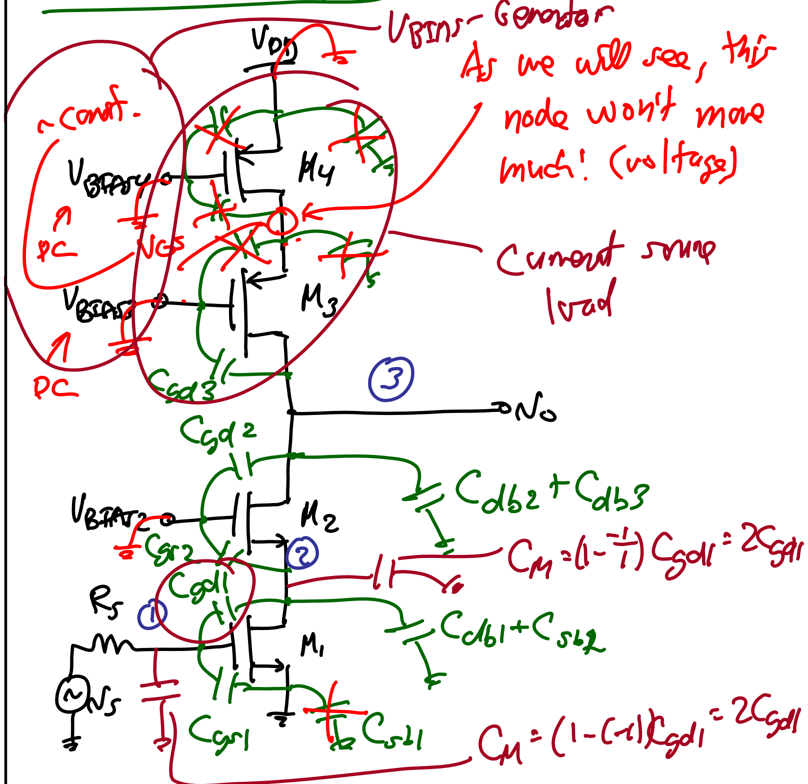
$$\frac{v_o}{v_s} = \frac{v_{①}}{v_s} \cdot \frac{v_{②}}{v_{①}} \cdot \frac{v_o}{v_{②}}$$

$$\frac{v_o}{v_s} = (1)\left(-g_{m1}\left(\cancel{\frac{1}{g_{m2}+g_{mb2}}}\right)\right)\left(\cancel{(g_{m2}+g_{mb2})}\, R_o\right)$$

$$= -g_{m1} R_o$$

same as C.S., but w/ R_o = huge!

Get the dominant pole: (w/ OCTC analysis)



$$\tau_{①} = (2C_{gd1} + C_{gs1}) R_s$$

$$\tau_{②} = (2C_{gd1} + C_{db1} + C_{sb2} + C_{gs2})\left(\frac{1}{g_{m2}+g_{mb2}}\right)$$

$$\tau_{③} = (C_{gd2} + C_{db2} + C_{db3} + C_{gd3}) R_o$$

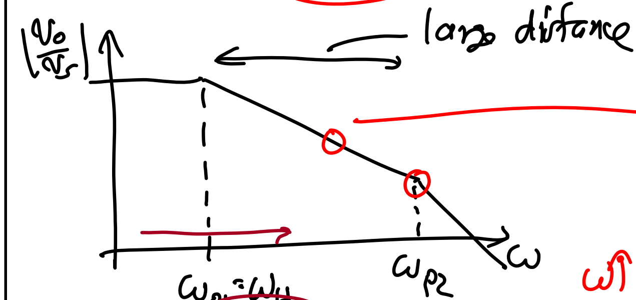
R_o ↑ huge!

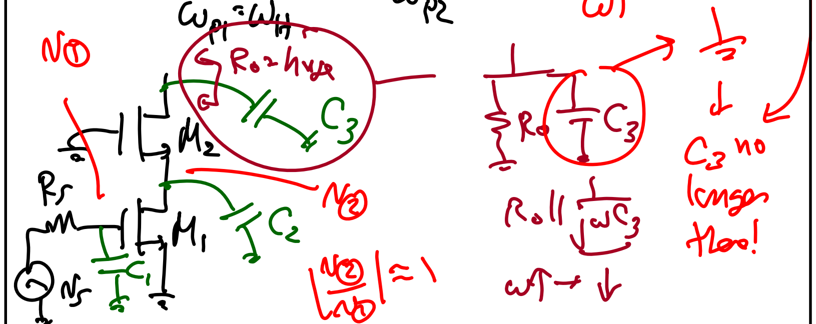
$$\boxed{\omega_H = \frac{1}{\tau_{①} + \tau_{②} + \tau_{③}}}$$

might need to include if R_s large

dominant!

$$\boxed{\omega_H = \frac{1}{\tau_{③}}}$$





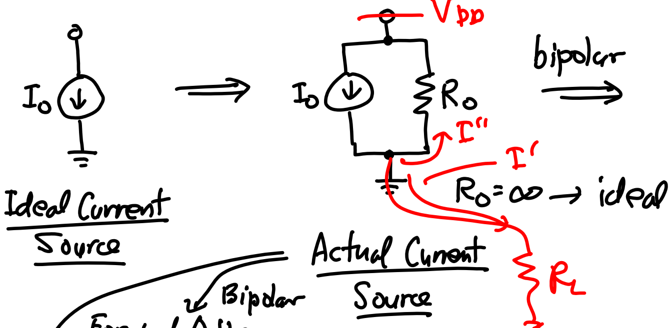
2nd pole (3rd pole),

$$\omega_{p2} = \frac{1}{\tau_1 + \tau_2}$$

over for Current Sources...

Transistor Current Sources

How can a transistor implement a current source?



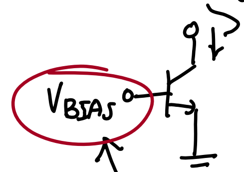
Ideal Current Source ⟹ Actual Current Source; bipolar ⟹

$R_o = \infty \rightarrow$ ideal

Bipolar: Forward-Active Xsistor Current Source

exponential

$$I_o = I_C = I_s \exp\left(\frac{V_{BIAS}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right)$$



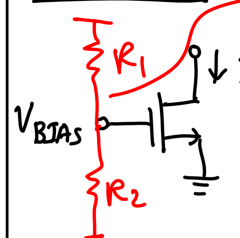
Very stable if V_{BIAS} = const. & V_A = large

Note that V_{BIAS} must be very accurate due to exponential → to several sig. figs.

e.g., $V_{BIAS} = 0.68745V$

MOS: Saturated MOS Xsistor Current Source

Can this really accurate to many sig. figs.?



$$I_o = I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{BIAS} - V_t)^2(1 + \lambda V_{DS})$$

Again, very stable if V_{BIAS} = const. & λ = small

Problem: need to generate a stable V_{BIAS}

We now focus on methods for generating V_{BIAS}.

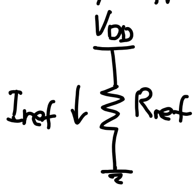
But how do we get this degree of precision using a transistor ckt?

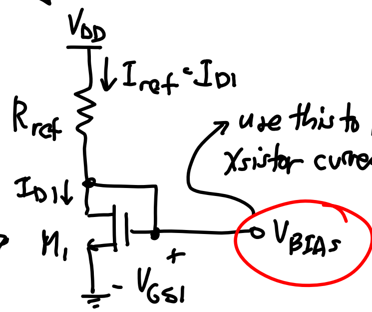
Solution: ↘

$\boxed{\text{Replica Biasing}}$ (a simple & effective approach)

1. Generate the desired current.
2. Push the current through a Xsistor and allow it to reach a stable bias pt.
3. Use this stable bias pt. as V_{BIAS} ← this can be very precise!

One simple approach:





use this to bias a Xsistor current source!

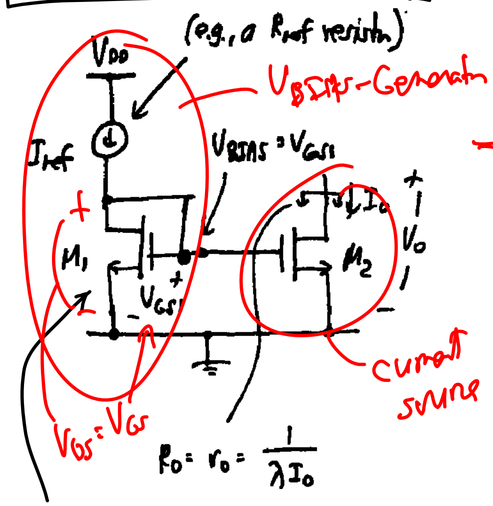
A diode connected Xsistor is always in saturation and will basically bias itself to support the needed current!

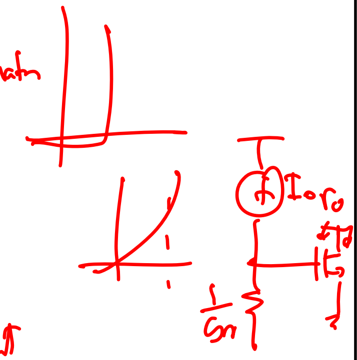
$$I_{ref} = I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_t)^2 (1 + \lambda V_{DS1})$$

↑ V_{BIAS}

Now, can distribute this V_{BIAS} to the gates of many MOS transistor current sources!

$\boxed{\text{Ex. Simple MOS Current Source}}$





$R_o = r_o = \frac{1}{\lambda I_o}$

Diode-connected Xsistor → saturation:

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{BIAS} - V_t)^2 (1 + \lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{BIAS} - V_t)^2 (1 + \lambda V_{DS2})$$

In general, $V_{DS1} \neq V_{DS2}$, but if λ = small, then little difference in I_{D1} & I_{D2}

① Case: matched M_1 & M_2 ⟹ $I_o = I_{ref}$

② Case: M_1 & M_2 scaled w.r.t. to each other

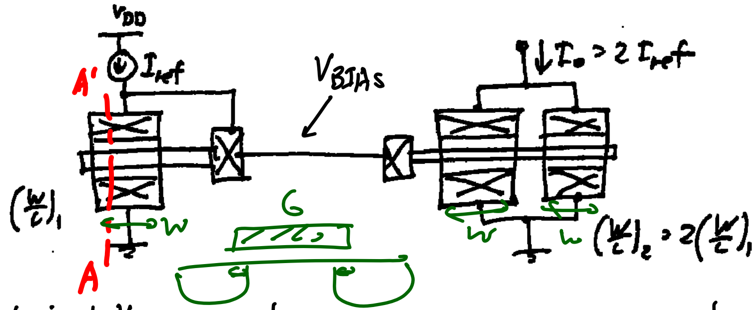
$$\Rightarrow \boxed{I_o = I_{ref}\frac{(W/L)_2}{(W/L)_1}}$$

⟹ use $L_1 = L_2$ for better accuracy, then:

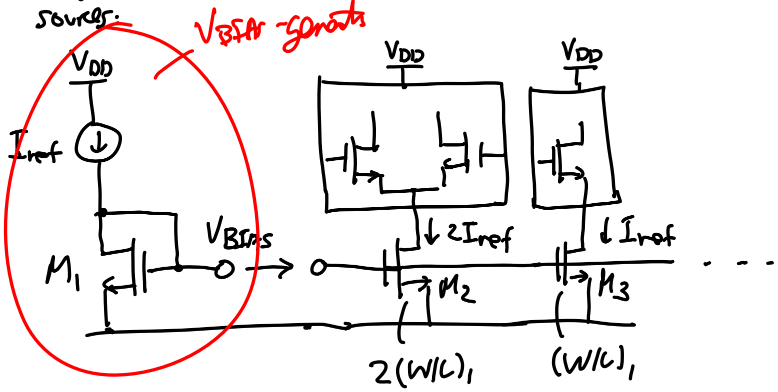
$$\boxed{\frac{I_o}{I_{ref}} = \frac{W_2}{W_1}}$$

Note: For better accuracy, should use multiple copies of one device when scaling currents → reduces edge effects!

Ex: Layout for a Doubling Current Source

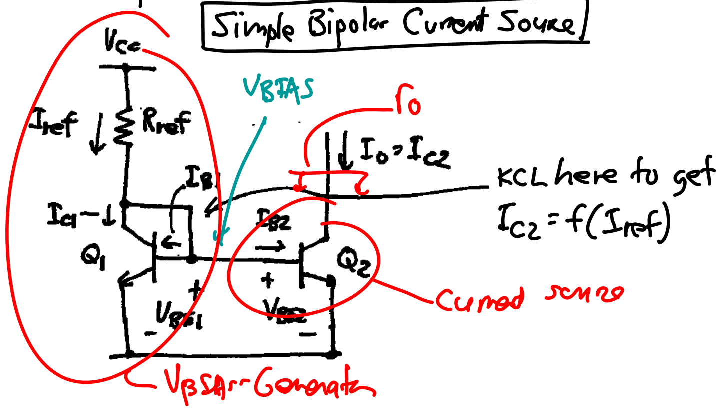


A single V_{BIAS} generator can now serve numerous current sources:



How about bipolar?

Simple Bipolar Current Source



Assume Q_1 & Q_2 are matched.

$V_{BE1} = V_{BE2} \longrightarrow I_{C1} = I_{C2} = I_o$ (neglecting V_A's) i.e., $V_A = \infty$

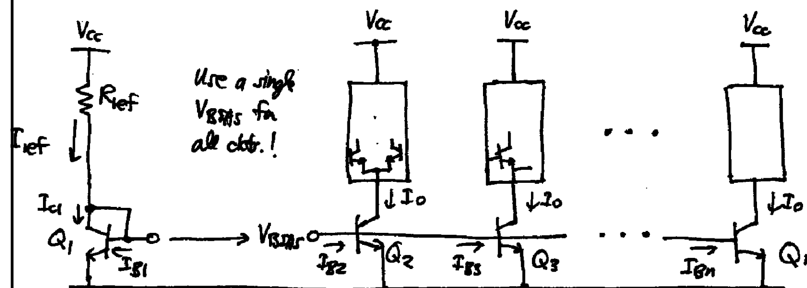
KCL: $I_{ref} = I_{C1} + I_{B1} + I_{B2} = I_{C1}\left(1 + \frac{2}{\beta}\right)$

$\therefore\ I_{C1} = I_{C2} = \boxed{I_o = \frac{I_{ref}}{1 + \frac{2}{\beta}}} \longrightarrow I_o \approx I_{ref}$

can say error $\sim \frac{2}{\beta}$

and $\boxed{I_{ref} = \frac{V_{CC} - V_{BE(on)}}{R_{ref}}}$ $\boxed{R_o = r_{o2}}$

Again, a single V_{BIAS} generator can serve many current sources throughout the IC chip:



$I_{ref} = I_{C1} + I_{B1} + I_{B2} + I_{B3} + \cdots + I_{Bn}$

[Identical Xistors] $\Longrightarrow$ $I_{ref} = I_{C1}\left(1 + \frac{n}{\beta}\right)$

$\Longrightarrow$ $\boxed{I_o = I_{C1} = \frac{I_{ref}}{\left(1 + \frac{n}{\beta}\right)}}$

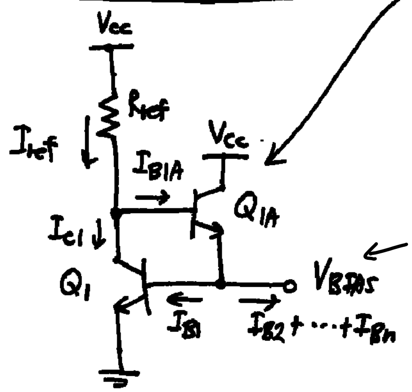
Problem: error $\sim \frac{n}{\beta}$ increases as n (I_o deviates from I_{ref}, and the deviation depends on n.)

This was not the case for MOS!

How can one reduce the error?

To reduce the error term, use a

$\boxed{\text{Buffered } V_{BIAS}\text{-Generator}}$



Add a buffer Xsistor to attenuate base currents from Xsistor current sources.

This can now drive the base currents of many bipolar transistor current sources (i.e., active loads).

$I_{ref} = I_{C1} + I_{B1A}$

$$I_{B1A} = \frac{I_{B1} + I_{B2} + \cdots I_{Bn}}{\beta+1} = \frac{n I_{C1}}{\beta(\beta+1)}$$

[Assuming identical Xsistors]

$$I_{ref} = I_{C1}\left(1 + \frac{n}{\beta(\beta+1)}\right)$$

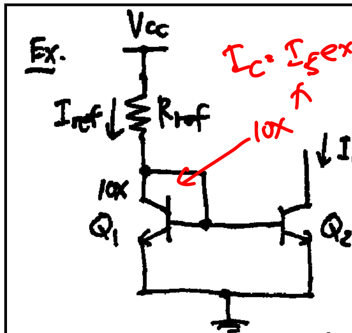
binomial approx.

$$\boxed{I_o = I_{C2} = \frac{I_{ref}}{1+\frac{n}{\beta(\beta+1)}} \approx I_{ref}\left(1 - \frac{n}{\beta^2}\right)}$$

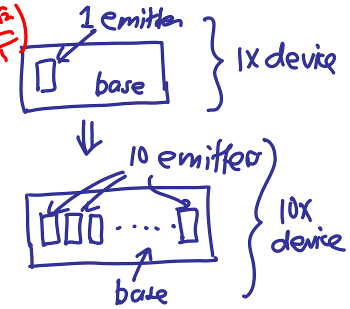
Note: Now, $\boxed{I_{ref} = \frac{V_{CC} - 2V_{BE(on)}}{R_{ref}}}$

Problem: For power savings reasons, oftentimes very small bias currents are needed, on the order of 5μA. This might force too large an R_{ref} in the above bipolar V_{BIAS} generator.

Ex.



$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$



i.e., larger emitter area: ↩ Layout like this to get more accurate ratio.

If Q_1 is 10x larger than Q_2.

$\therefore I_{S1} = 10 I_{S2} \rightarrow I_o \cong I_{ref}/10$

$$\therefore I_o = \frac{(V_{CC} - V_{BE(on)})}{10 R_{ref}} \rightarrow R_{ref} = \frac{V_{CC} - V_{BE(on)}}{10 I_o}$$

this helps to lower R_{ref}, but is it enough?

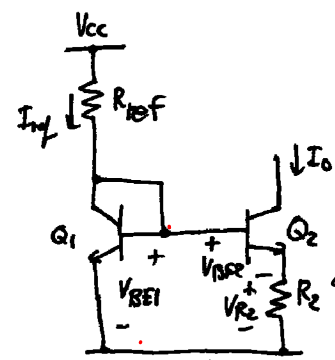
Ex. $I_o = 5\mu A$, $V_{CC} = 30V$

$R_{ref} \cong \frac{30}{5\mu} = 600k\Omega$ ← That's way too big! (Yes, there's only one of them on the chip, but this takes up too much space!)

The Low Current Solution: $\boxed{\text{Widlar Current Source}}$

⟹ scale $I_{C2} = I_o$ by reducing V_{BE2} (relative to V_{BE1}):

Do this by emitter degenerating Q_2 via R_2



$I_{C2} = I_{S2} \exp\left(\frac{V_{BE2}}{V_T}\right) < I_{C1}$

$$V_{BE1} = V_{BE2} + V_{R_2} = V_{BE2} + \frac{1}{\alpha} I_{C2} R_2 \approx V_{BE2} + I_{C2} R_2$$

$$I_{C2} R_2 = V_{BE1} - V_{BE2} = V_T \ln \frac{I_{C1}}{I_{S1}} - V_T \ln \frac{I_{C2}}{I_{S2}}$$

$$I_{C2} R_2 = V_T \ln \frac{I_{C1}}{I_{C2}}$$ [Assuming Q_1 & Q_2 are matched.]

$$\boxed{I_o R_2 = V_T \ln \frac{I_{ref}}{I_o}}$$

Rule of Thumb:

$V_{R_2} = I_{C2} R_2$	$I_{C2} = I_o$
18mV	$\frac{1}{2} I_{ref}$
42mV	$\frac{1}{5} I_{ref}$
60 mV	$\frac{1}{10} I_{ref}$
120 mV	$\frac{1}{100} I_{ref}$

5μA example again

Ex. scale by 100X using Widlar source

$V_{BE1} - V_{BE2} = 120\text{mV} \rightarrow R_2 = \frac{120\text{mV}}{5\mu A} = \underline{24k\Omega}$

$I_{ref} = 500\mu A \rightarrow R_{ref} = \frac{30V}{500\mu A} = \underline{60k\Omega}$

More reasonable than 600kΩ before.
If want smaller, scale by 1000X instead.

Another advantage of the Widlar: larger R_o ∴ a more ideal current source:

$$R_o = r_{o2}(1 + g_{m2} R_2)$$