Lecture 16: Slew Rate & Output Stages

- Announcements:
  - Midterm will be on the date specified in your syllabus: Thursday, March 21, 3:30-5 p.m. in 390 Hearst Mining Building
  - No lecture the day of the midterm
  - HW#7 due tomorrow
  - HW#8 will be available today and due Tuesday next week (I know, but this will help you on the midterm)
  - Passed out midterm info sheet with past 3 exams from (my) EE140
- Lecture Topics:
  - Compensation (a 1st pass)
  - Slew Rate
  - Output Stages
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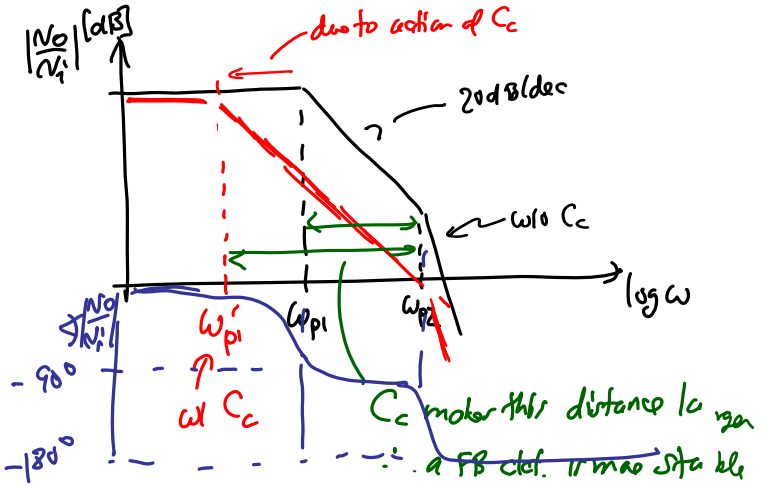
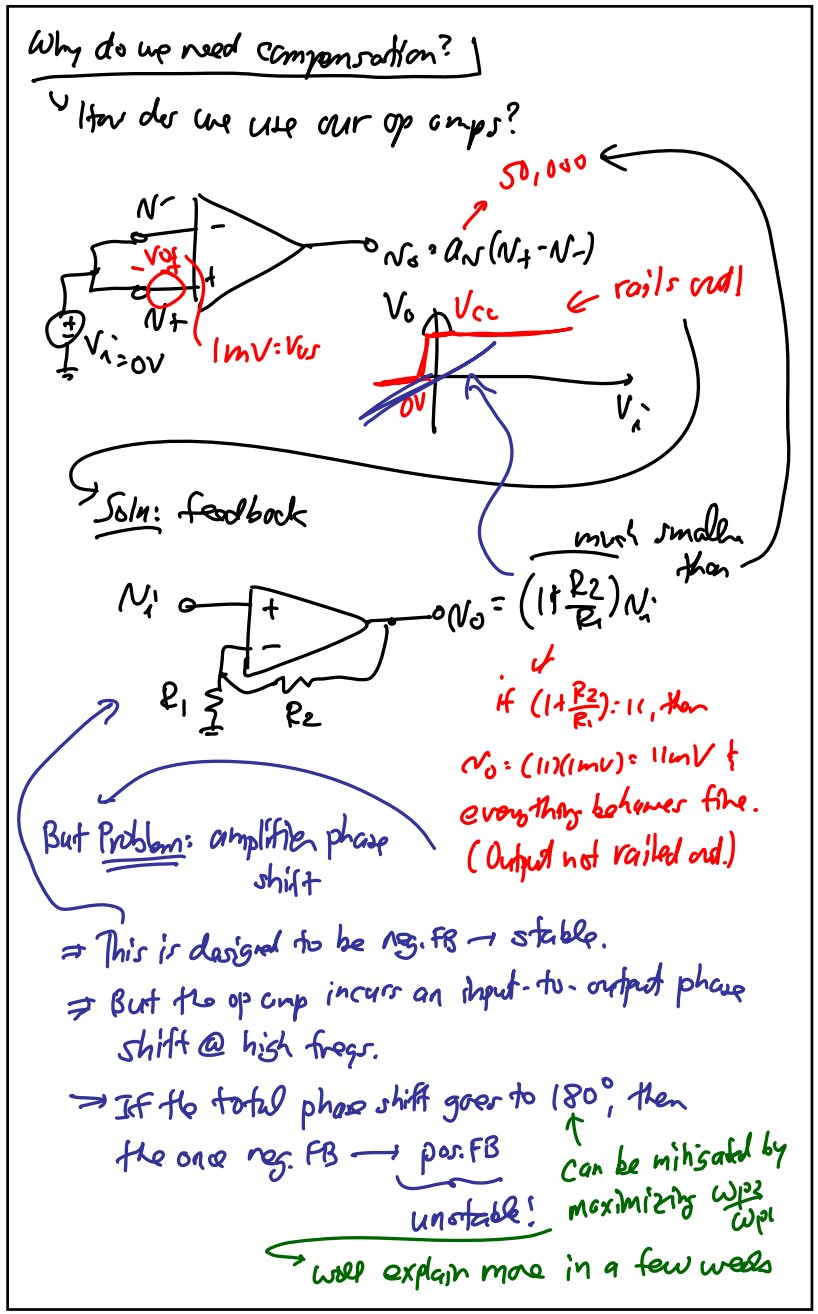
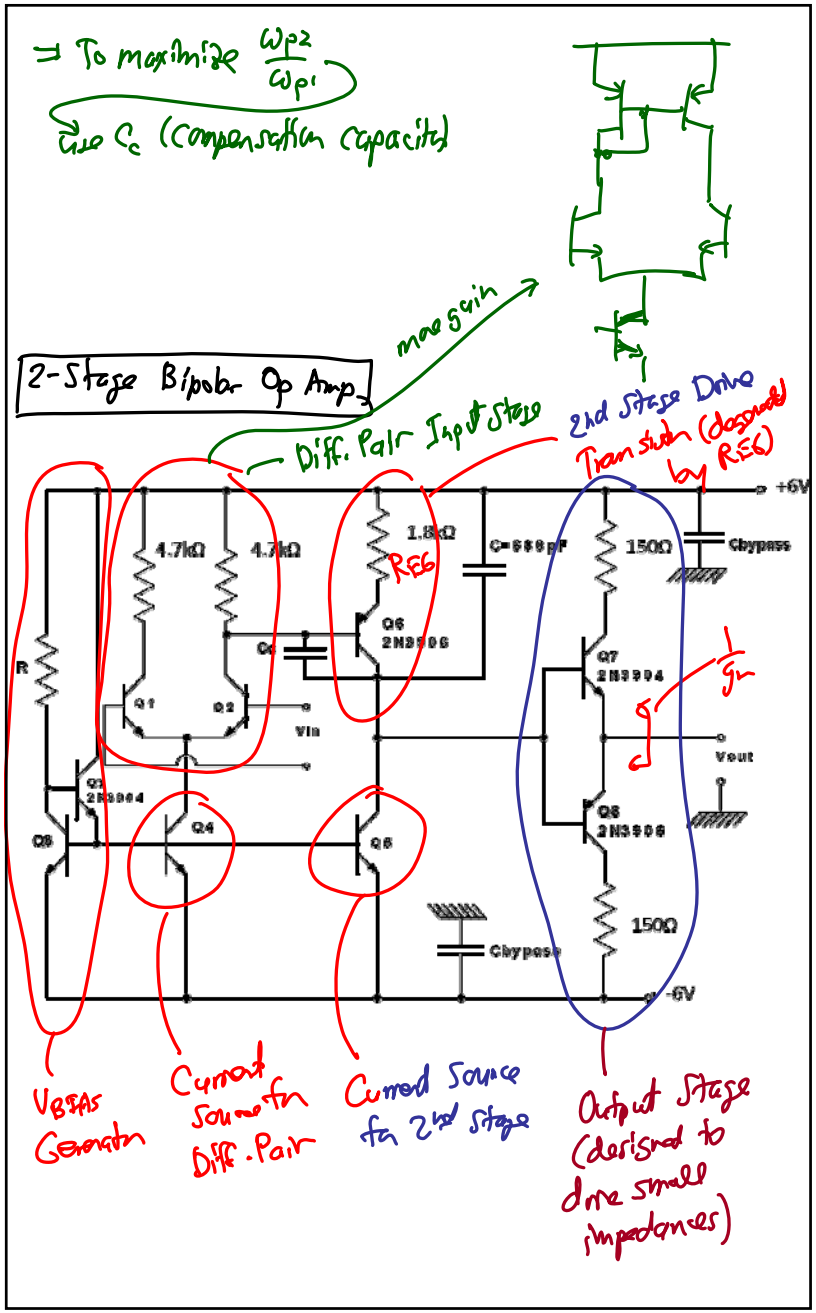
- Last Time:
- Compensation: a first pass







Remarks.

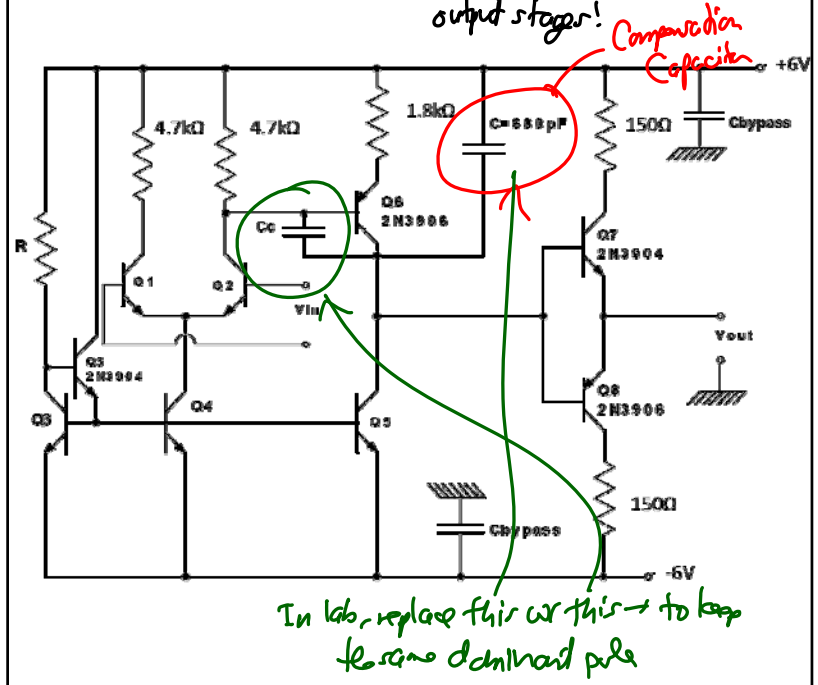
① You analyze this in Lab #2.

② Usually, the resistively-loaded diff. pair is replaced w/ an active current mirror load for more gain.

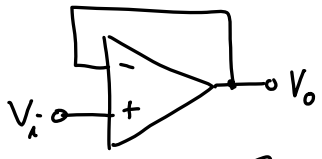
③ R_{EG} raises the input R of Q_6 (of the 2nd gain stage), plus helps w/ biasing.

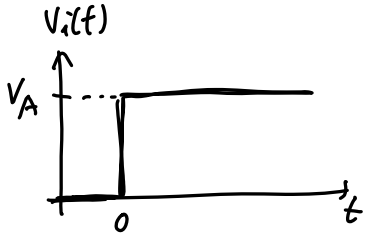
④ Same comment as ③ for the output stage.

⑤ Output stage needed when driving a resistive load
↳ often the case for bipolar
↳ not often the case for MOS, where a capacitive load C_L is often more relevant → MOS op amps often don't need output stages!



Slew Rate





Using Laplace Xform Theory:

$$\frac{V_o}{V_i}(s) = \frac{1}{1+\frac{s}{\omega_1}} = \frac{1}{1+s\tau_1}$$

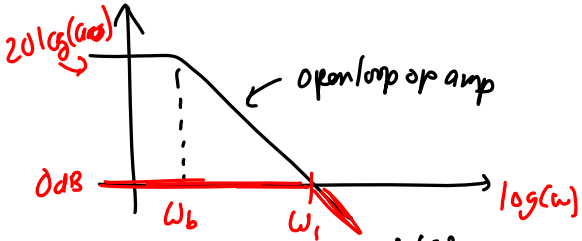
↖ single (dominant) pole

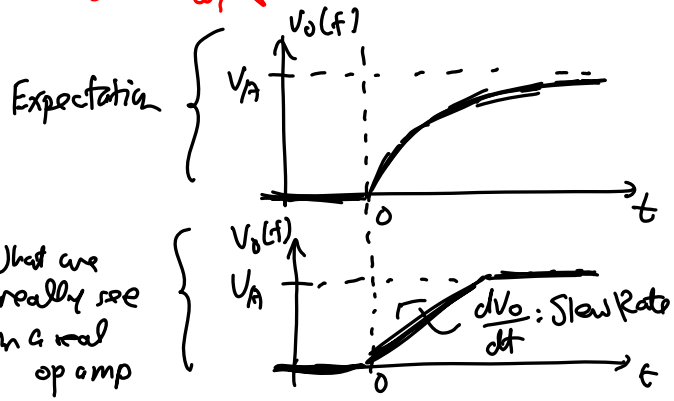
$$V_i(s) = \frac{V_A}{s}$$

$$V_o(s) = \frac{V_A}{s(1+s\tau_1)} = \frac{V_A}{s} - \frac{V_A}{s+\frac{1}{\tau_1}}$$

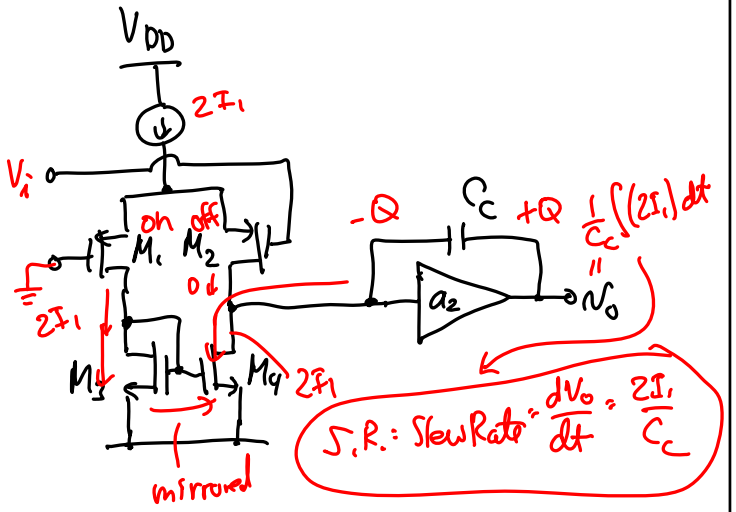
⇕ Inverse Laplace Xform

$$V_o(t) = V_A(1-e^{-t/\tau_1})$$ ← expected response

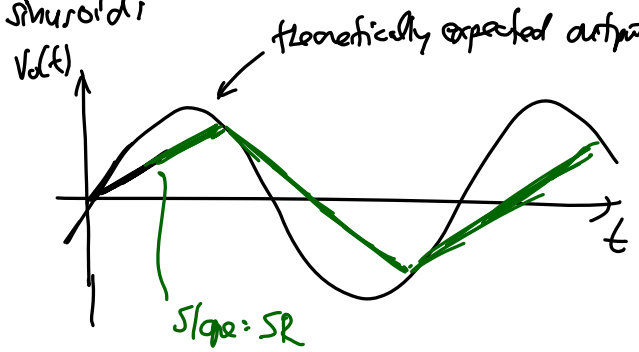




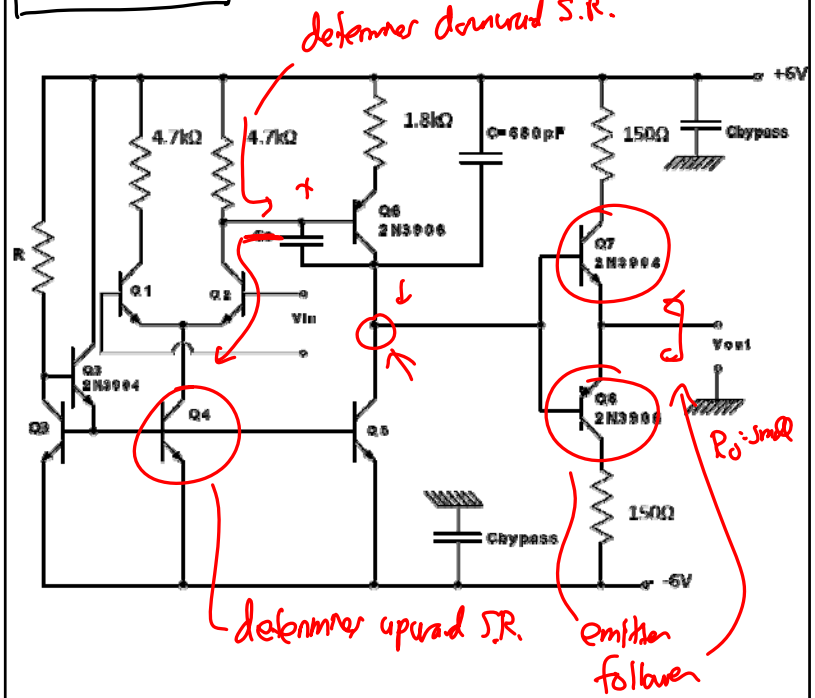
Reason: 1st or 2nd stage of op amp cannot source enough current to mimic the slope (or speed) of a fast rising input signal



If apply a very fast (i.e., high frequency), large amplitude sinusoid:



Lab Slew Rate



Output Stages

- Class A (Emitter or Source Follower)
- Class B
- Class AB (we'll do this one later)

Purpose: Drive loads

① Deliver power w/ small distortion.

② Minimize output impedance → so that the amplifier gain is insensitive to the load.

Desirable Attributes:

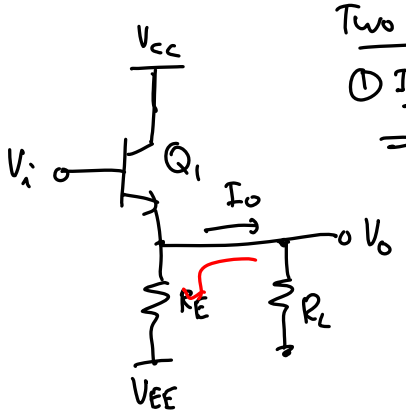
① High R_{in}; Low R_{out}.

② Low quiescent power.

③ Minimal effect on the amplifier freq. response.

④ Should be able to handle large input/output swings. (i.e., V_i may be $> V_T$, invalidating small-signal approximations)

Emitter Follower (Class A)



Two main cases:

① $I_o > 0$: I_o comes from Q_1

⇒ adequate I_o can be supplied so long as Q_1 stays forward-active

② $I_o < 0$: (i.e., V_o : (-1)

I_o must be sunk through R_E to V_{EE}.

I_o: $\frac{V_o - V_{EE}}{R_E}$ → I_o gets smaller as V_o ↓