Lecture 22: CMOS Op Amp Compensation

- **Announcements:**
- This lecture will be 2 hours (3rd lecture to make up for missing Tuesday)
- As mentioned, I unfortunately need to miss the Thursday lecture
- So next three lectures will also be 2 hours, with video of at least the last half hour posted online
- Design Project Checkpoint:
  - Due Monday, April 22, 11:59 p.m.
  - Send to your TA a spice file for your op amp design that simulates correctly, i.e., that reaches a stable bias point where all transistors are saturated (or linear if an MOS resistor)
  - It doesn't need to meet the project specs, but it should simulate correctly
- **Lecture Topics:**
  - Review of Pole-Zero Plots
  - Practical CMOS Op Amp Compensation
  - Nulling the RHP Zero
- -----------------------------------
- **Last Time:**
- Brute force analyzed a two-stage CMOS op amp
- Continue with this now …

over

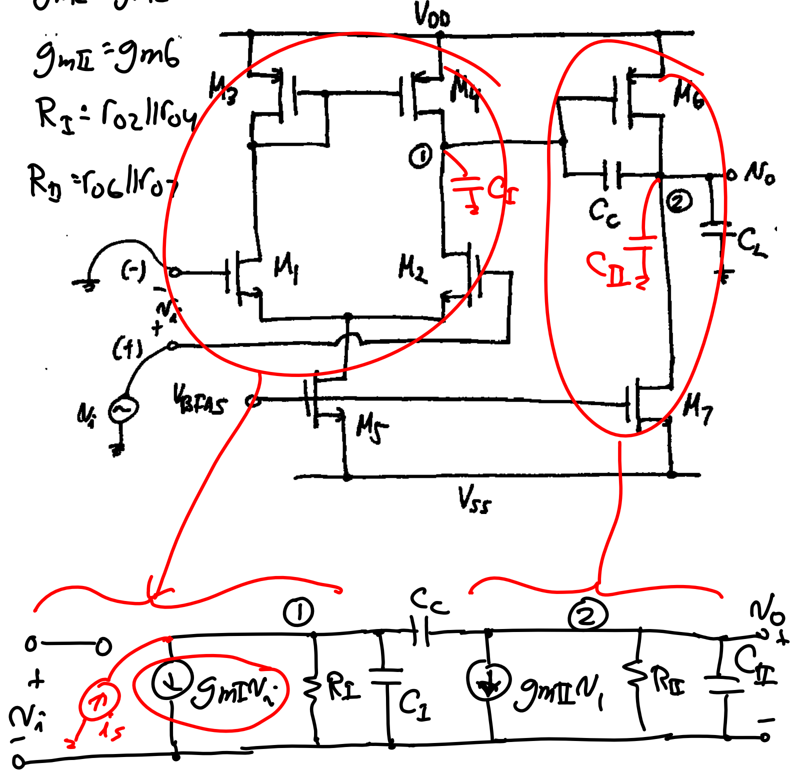
CMOS 2-Stage Op Amp Compensation

$g_{mI} = g_{m2}$

$g_{mII} = g_{m6}$

$R_I = r_{o2} \| r_{o4}$

$R_{II} = r_{o6} \| r_{o7}$



KCL①: $i_s = \frac{v_1}{R_I} + sC_I v_1 + (v_1 - v_o)sC_c$

KCL②: $g_{mII}v_1 + \frac{v_o}{R_{II}} + sC_{II}v_o + (v_o - v_1)sC_c = 0$

$$\frac{v_o}{i_s} = \frac{\overbrace{(g_{mII} - sC_c)R_I R_{II}}^{N(s)}}{\underbrace{1 + s\left[(C_{II}+C_c)R_{II} + (C_I+C_c)R_I + g_{mII}R_I R_{II} C_c\right] + s^2 R_I R_{II}(C_I C_{II} + C_c C_I + C_c C_{II})}_{D(s)}}$$

$$\frac{v_o}{i_s}(s) = \frac{N(s)}{D(s)}$$ → This xfer fcn has 2 poles & one zero.

The zero: $N(s) = 0 \rightarrow$ ($z = s$) $\quad z = \dfrac{g_{mII}}{C_c}$ ← (+) & real

The poles:

$$D(s) = \left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right) = 1 - s\left(\frac{1}{p_1} + \cancel{\frac{1}{p_2}}\right) + \frac{s^2}{p_1 p_2}$$

negl.

$[p_2 \gg p_1] \rightarrow \approx 1 - \dfrac{s}{p_1} + \dfrac{s^2}{p_1 p_2}$

i.e., there is a dominant pole

Thus:

$$p_1 = -\frac{1}{(C_{II}+C_c)R_{II} + (C_I + C_c)R_I + g_{mII} R_I R_{II} C_c}$$

→ As $C_c\uparrow \rightarrow p_1\downarrow$

$$\approx -\frac{1}{g_{mII} R_I R_{II} C_c} = p_1$$

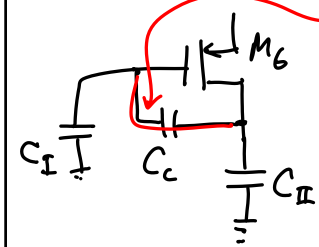
For the 2nd pole:

$$p_1 p_2 = \frac{1}{R_I R_{II}(C_I C_{II} + C_c C_I + C_c C_{II})}$$

$$p_2 = -\frac{g_{mII} C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \xrightarrow{\text{As } C_c\uparrow} \simeq \boxed{p_2 = -\frac{g_{mII}}{C_I + C_{II}}}$$

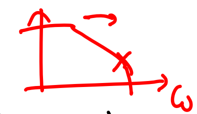
$C_c\uparrow \rightarrow p_2\uparrow$

ω_2 By Inspection



When $C_c\uparrow$, it becomes a short at high freqs. & M_6 becomes "diode-connected"

$$\omega_2 = \frac{1}{\tau} = \frac{1}{\left(\frac{1}{g_{m6}}\right)(C_I + C_{II})} = \frac{g_{mII}}{C_I + C_{II}} \checkmark$$



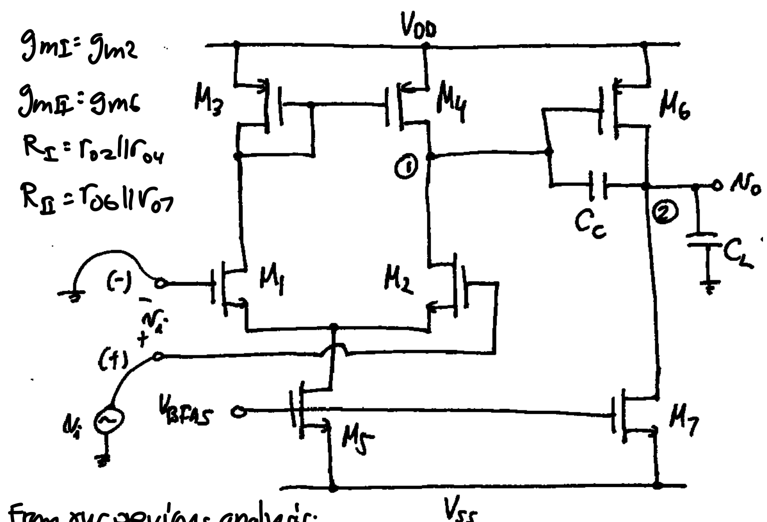
CMOS 2-Stage Op Amp Compensation (Summary)

$g_{mI} = g_{m2}$

$g_{mII} = g_{m6}$

$R_I = r_{o2} \| r_{o4}$

$R_{II} = r_{o6} \| r_{o7}$



From our previous analysis:

$$p_1 = -\frac{1}{g_{mII} R_I R_{II} C_c}$$

$[C_c \gg C_I \text{ or } C_{II}]$ $\quad [C_L \gg C_I]$

$$p_2 = -\frac{g_{mII} C_c}{C_I C_{II} + C_c(C_I + C_{II})} \approx -\frac{g_{mII}}{C_I + C_{II}} \approx -\frac{g_{m6}}{C_L}$$

$$z = +\frac{g_{mII}}{C_c}$$ ← RHP zero (this will cause problems)

Remarks:

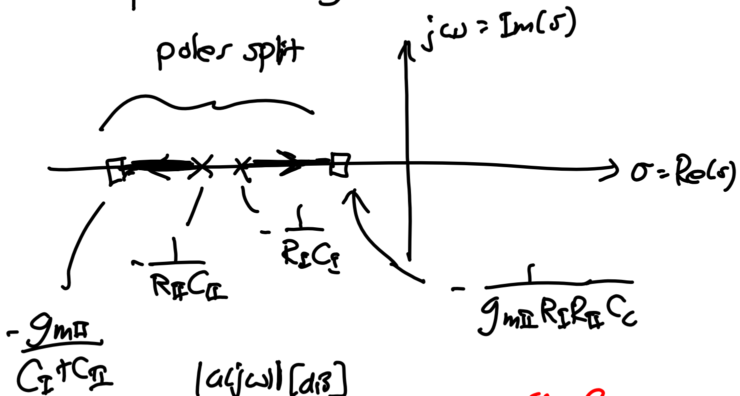
① Note that as $C_c \uparrow \rightarrow |p_1| \downarrow$

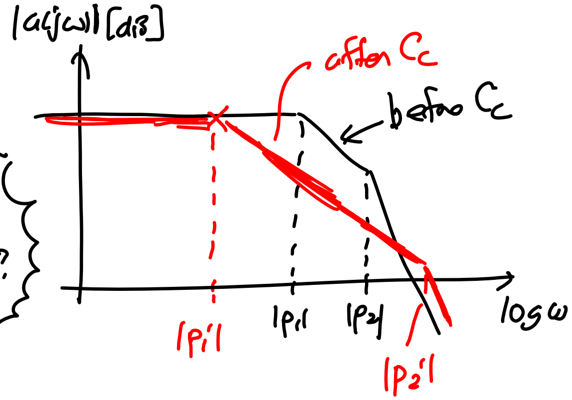
② As $C_c \uparrow \rightarrow |p_2| \uparrow \rightarrow |p_2| = \dfrac{g_{mII}}{C_I + C_{II}}$

③ With $C_c = 0$ (i.e., before compensation)

$$p_1 = -\frac{1}{R_I C_I} \qquad p_2 = -\frac{1}{R_{II} C_{II}}$$

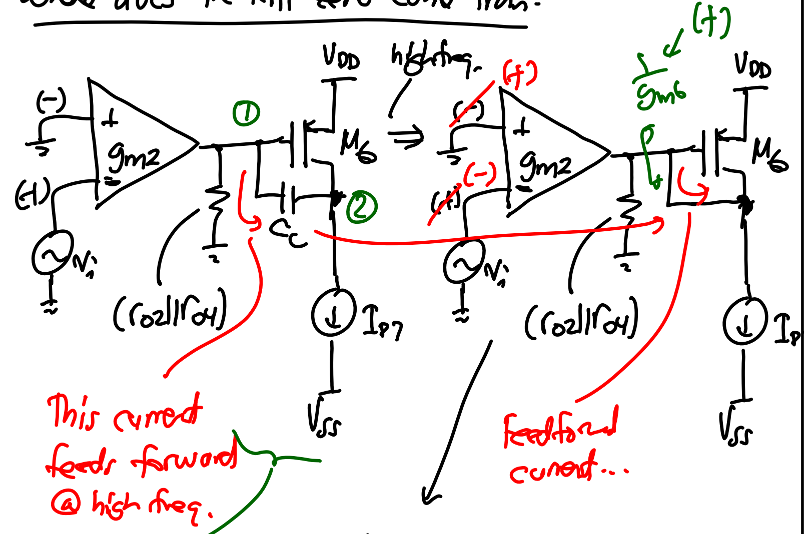
④ On a pole/zero diagram:





But what about the RHP zero?

Where does the RHP zero come from?

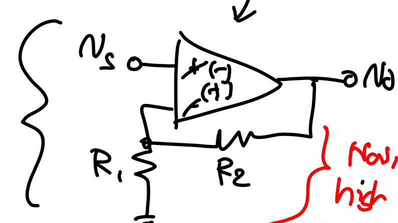


$$\frac{v_{②}}{v_{①}} = -g_{m6}(r_{o6} \| r_{o7})$$

(−)!

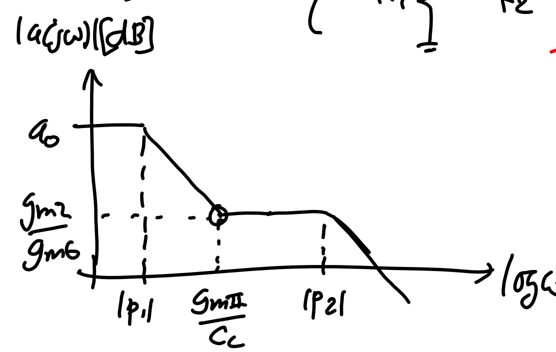
$$\underbrace{\frac{v_o}{v_i} = -\frac{g_{m2}}{g_{m6}}}$$

Negative! Should be (+)!



Unstable!

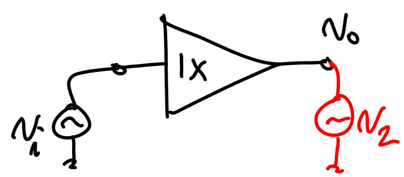
Now, @ high freq., have (+) FB!



Observation.

The Miller effect for compensation requires the FB path. → BUT: the feedforward path (that causes the zero) is not needed!

Solution: ① Kill the feedforward path.
② Keep the feedback path.



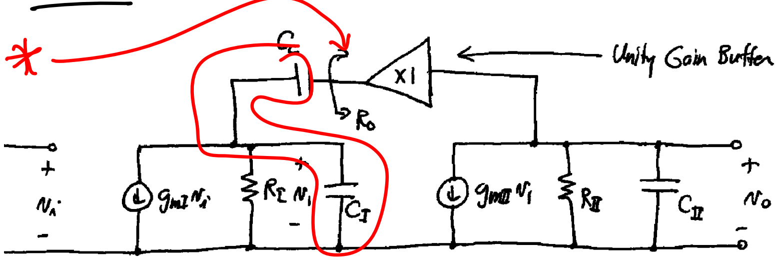
$\frac{v_o}{v_i} \approx 1$

$\frac{v_i}{v_2} \ll 1$

∴ buffer is directional

Put in series w C_c → do this

The Ckt:



Apply KCL: $p_1 \cong -\frac{1}{g_{mII} R_I R_{II} C_c}$ (same as before)

$$p_2 \cong -\frac{g_{mII} C_c}{C_{II}(C_I + C_c)} \underset{[C_c \gg C_I]}{\cong} -\frac{g_{mII}}{C_{II}}$$

$$p_3 \cong \frac{-1}{R_o \underbrace{(C_I C_c/(C_I + C_c))}_{\text{series combination of } C_I \,\&\, C_c}} \underset{[C_I \ll C_c]}{\cong} -\frac{1}{R_o C_I}$$

comes from this node → *

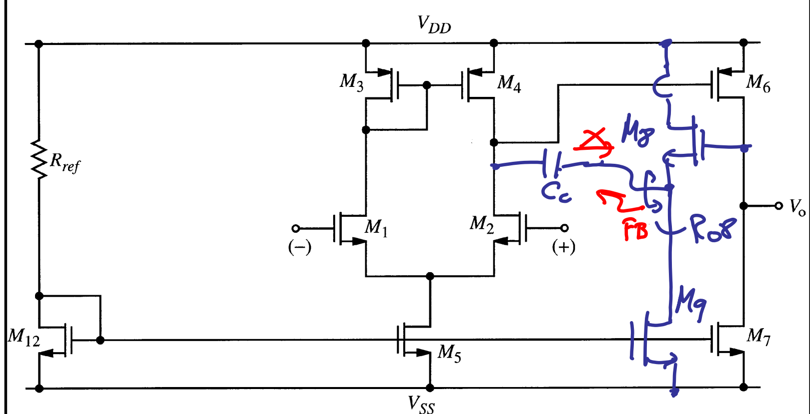
$$z_2 \cong -\frac{1}{R_o C_c} \leftarrow \text{LHP zero! Good!}$$

Remarks.

① An additional pole $p_3 = -\frac{1}{R_o C_I}$ has been created! But since R_o: small (for a buffer) and C_I: small, p_3 is at a very high freq. → contributes very little phase @ ω_{ulg}, where $|T(j\omega)| = 1$.

② A LHP zero now emerges, $z_I = -\frac{1}{R_o C_c}$.
This helps stability as discussed before. (by contributing (+) phase shift → PM↑)

Actual Implementation of Buffer-Based Zero Cancellation

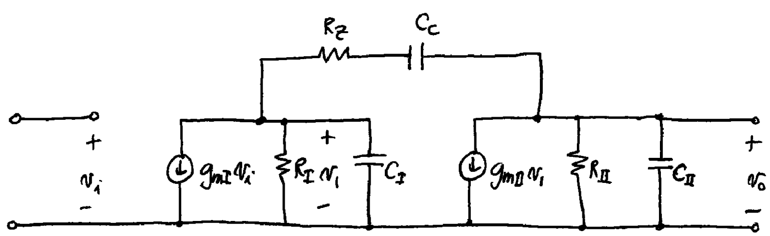


$R_{o8} = \frac{1}{g_{m8}} = \frac{1}{\sqrt{2\mu_n C_{ox}(W/L)_8 I_{D8}}}$ → want this sufficiently small to drive $|p_3|\uparrow$

Thus, need: ① $(W/L)_8\uparrow$
② $I_{D8}\uparrow$

Don't like for size & power consumption reasons.

Solution: $\boxed{\text{Nulling Resistor in Series w/ } C_c}$



Doing KCL:

$$p_1 \cong -\frac{1}{g_{mII}R_I R_{II} C_c}$$

$$p_2 \cong -\frac{g_{mII}C_c}{C_I C_{II} + C_c(C_I + C_{II})} \approx -\frac{g_{mII}}{C_{II}}$$

Same as before

$$p_3 = -\frac{1}{R_z C_I} \quad \leftarrow \text{pole due to } R_z$$

$$z_1 = \frac{1}{C_c\left(\frac{1}{g_{mII}} - R_z\right)} \quad \leftarrow \text{relocated zero (function of } R_z)$$

Note: The position of the zero depends upon the value of the "nulling resistor" R_z

If $R_z < \frac{1}{g_{mII}}$, then z_1 is in the RHP ✗

If $R_z > \frac{1}{g_{mII}}$, then z_1 " " " LHP ✓

This is great! → Can convert the zero to a LHP zero!

Can even stick the zero on top of a pole!

$$H(s) = \cdots \frac{\cancel{(s - z_1)}}{\cancel{(s - p_1)}}$$

If $z_1 = p_1$

much better PM...

The Root Locus: