Lecture 24-25: Settling Time, PSRR, Feedback

- **Announcements:**
- This lecture will be 2 hours (2nd lecture to make up for missing Thursday)
- Video of last half hour will be posted
- Next lecture will also be 2 hours, with video of at least the last half hour posted online
- HW#11 due tomorrow
- HW#12 online soon
- **Lecture Topics:**
  - Settling Time
  - Power Supply Rejection Ratio (PSRR)
  - Advantages of Feedback (revisited)
  - Feedback Configurations
  - Effect of FB on Z_i and Z_o
- ----------
- **Last Time:**

$$SR = \frac{dV_o}{dt} = \frac{I_{xm}}{C_c} = \frac{I_{xm}}{G_{m1}}\omega_{ugf}A_0 = SR$$

$$C_c = \frac{G_{m1}}{\omega_{ugf}A_0}$$

$\omega_{ugf} = \omega$ @ $|a(j\omega)f| = 1$

To Increase SR:

1. Decrease G_{m1} ← transconductance of 1st stage
2. Increase ω_{ugf} ← increase ω_2; limited by the existing freq. range
3. Use a larger A_0, if possible.

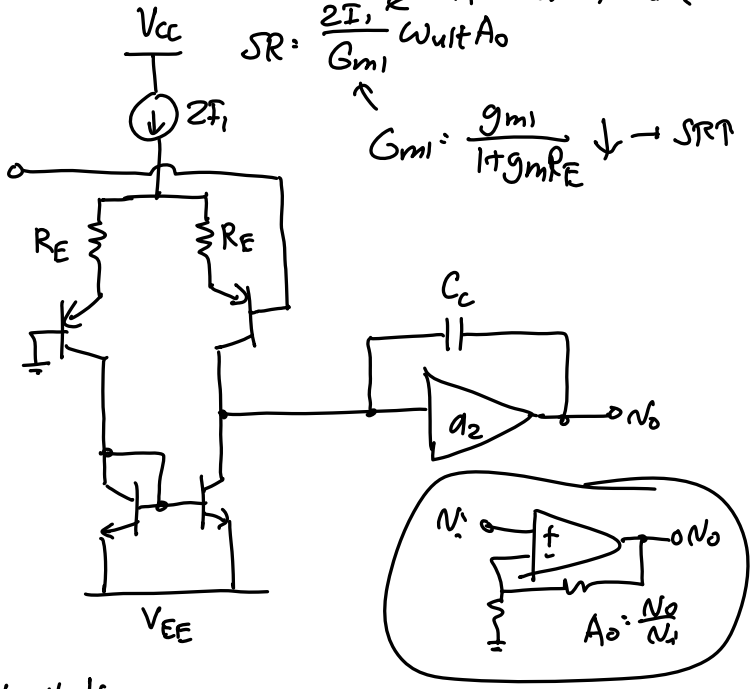
Increasing SR via G_m-Reduction

1. Emitter or Source Degeneration @ the Input Stage:

I_1 remains the same

$$SR = \frac{2I_1}{G_{m1}}\omega_{ugf}A_0$$

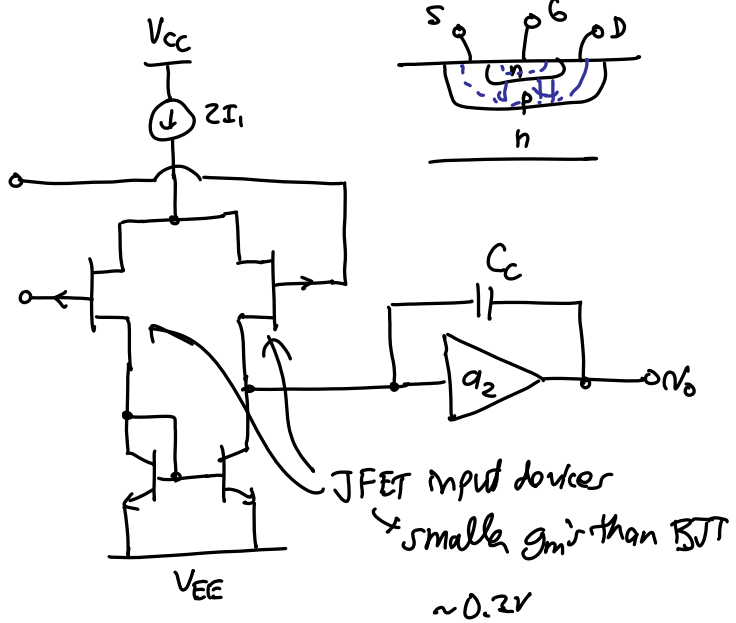
$$G_{m1} = \frac{g_{m1}}{1+g_{m1}R_E} \downarrow \rightarrow SR\uparrow$$



Limitations:

1. R_E mismatch → $V_{OS}\uparrow$
   ↳ must limit value of R_E to limit V_{OS}
2. $R_E\uparrow$ → gain↓ (SR-gain trade-off)
3. R_E contributes noise (thermal)

② FET Input Devices –



JFET input devices
↳ smaller g_m's than BJT

For FET's: $\frac{g_m}{I_D} \cong \frac{2}{V_{GS}-V_t}$ ← ~0.2V

For BJT's: $\frac{g_m}{I_C} = \frac{1}{V_T}$ ← ~26mV

$$\frac{\text{FET SR}}{\text{BJT SR}} = \frac{\frac{I_D}{g_{mF}}\omega_{ult}}{\frac{I_C}{g_{mB}}\omega_{ult}} = \frac{\frac{V_{GS}-V_t}{2}}{V_T} = \frac{V_{GS}-V_t}{2V_T} \approx \frac{260}{26} \approx 10$$

Limitations:
① Higher V_{OS}
② Increased voltage noise. (but decreased current noise)

Settling Time

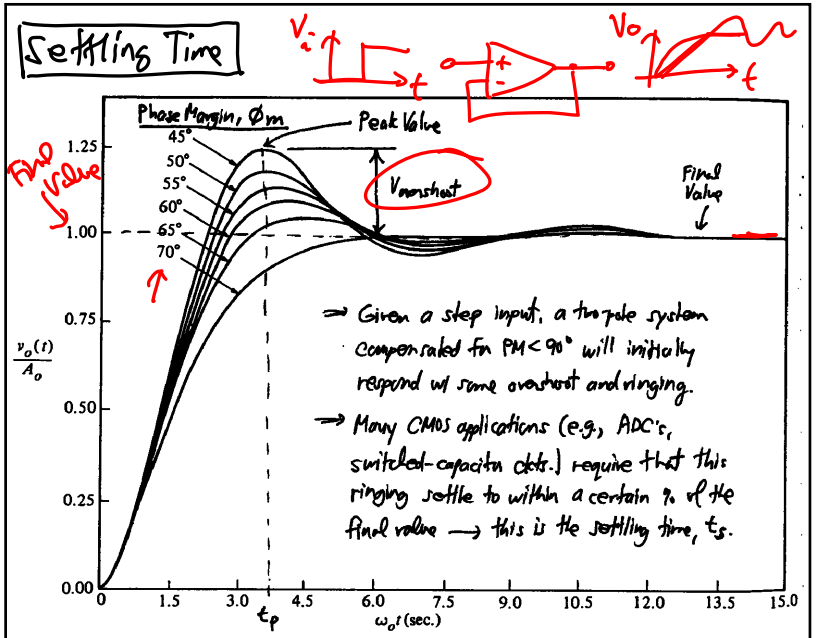
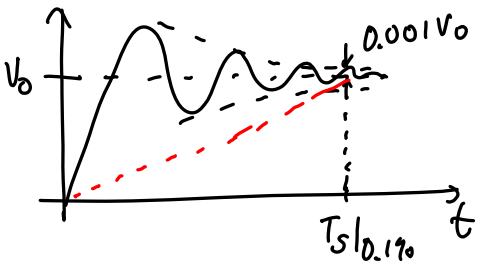


Figure 8.2-3 Response of second-order system with various phase margins.

Obtain Expressions for:
① $V_{overshoot}$ ←
② Settling Time, T_s ←
} as functions of phase margin, ϕ_m

- Go through settling time handout

Rule of Thumb for Lab (Project)

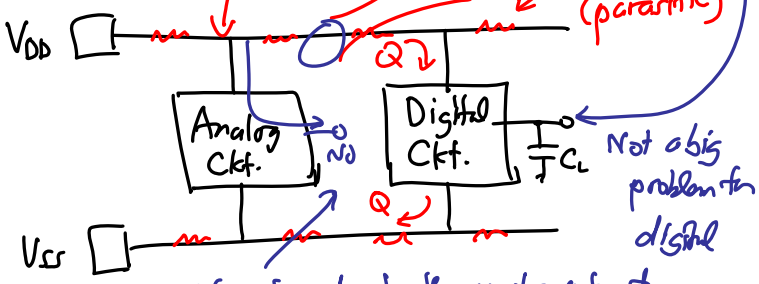


$SR \sim \frac{V_o}{\left(\frac{T_s|_{0.1\%}}{10}\right)}$

$SR \sim \frac{10V_o}{T_s|_{0.1\%}}$

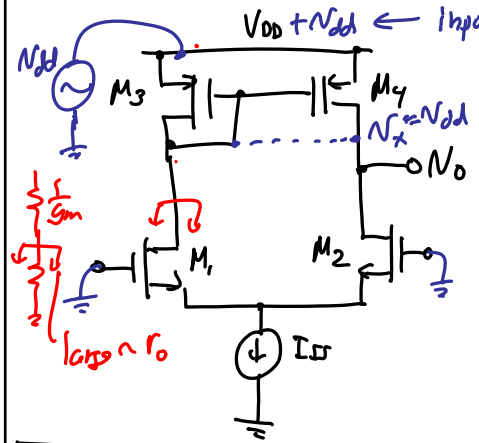
Power Supply Rejection Ratio (PSRR)

In today's mixed-signal ckts:



If noise gets to the analog output → BIG PROBLEM!

Ex. CMOS Differential Input Stage w/ Current Mirror Load



Thus:

$\frac{N_0}{N_{dd}} \approx 1$ → supply noise directly reaches the output!

Definition. Power Supply Rejection Ratio (PSRR)

$$PSRR \triangleq \frac{\text{Gain f/ Input to Output}}{\text{Gain f/ Supply to Output}} = \frac{A_V|_{V_{dd}=0}}{A_{dd}|_{V_i=0}}$$

Thus, for the above example:

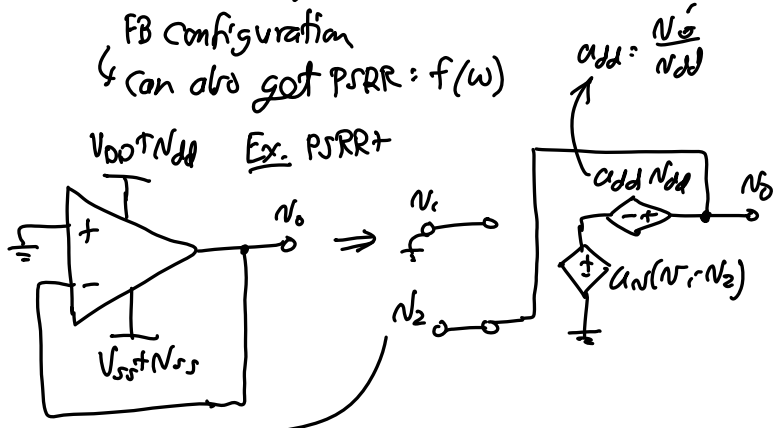
$$PSRR = \frac{g_{m2}(r_{o2}\|r_{o4})}{1} \Rightarrow \boxed{PSRR \approx g_{m2}(r_{o2}\|r_{o4})}$$

For more complicated circuits, much more work is involved

↳ to make things easier, use a unity gain FB configuration

↳ can also get PSRR = f(ω)

Ex. PSRR+



$$N_0 = a_V(N_i - N_2) + a_{dd}N_{dd}$$

$-N_0$

$$N_0(1+a_V) = a_{dd}N_{dd}$$

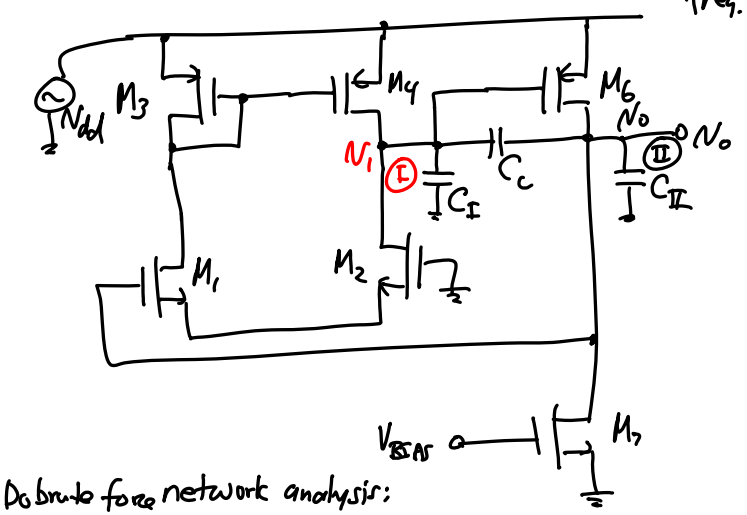
$$\frac{N_0}{N_{dd}} = \frac{a_{dd}}{1+a_V} = \frac{1}{\frac{1}{g_{dd}} + \frac{a_V}{a_{dd}}} \approx \boxed{\frac{1}{PSRR+} = \frac{N_0}{N_{dd}}}$$

Just find the xfer fcn to PSRR+ when the op amp is hooked into unity gain FB

$$\boxed{PSRR+ = \frac{N_{dd}}{N_0}}$$

Two-Stage Op Amp PSRR+

Want PSRR+ = f(ω) (ω: freq.)



Do brute force network analysis:

KCL(I): $G_I N_{dd} = (G_I + sC_c + sC_I) N_1 - (g_{mI} + sC_c) N_o$

KCL(II): $(g_{mII} + g_{ds6}) N_{dd} = (g_{mII} - sC_c) N_1 + (G_{II} + sC_c + sC_{II}) N_o$

$G_I = g_{ds1} + g_{ds4} = g_{ds2} + g_{ds4}$

$G_{II} = g_{ds6} + g_{ds7}$

$g_{mI} = g_{m1} = g_{m2}$

$g_{mII} = g_{m6}$

$[g_{ds} = \frac{1}{r_o}]$ ← For saturated device.

math & rearranging

Get: $\left.\frac{N_{dd}}{N_o}\right|_{closed\text{-}loop} = \frac{N(s)}{D(s)} = \frac{(\quad)}{(\quad)}$ polynomials

↳ then use: $N(s) = 1 + \left(\frac{s}{z_1} + \frac{s}{z_2}\right) + \frac{s^2}{z_1 z_2} \approx 1 + \frac{s}{z_1} + \frac{s^2}{z_1 z_2}$

$$PSRR^+ = A_{No}^+ \left[\frac{\left(1+\frac{s}{GB}\right)\left(1+\frac{s}{|p_2|}\right)}{\left(1+\frac{s}{GB/A_{No}^+}\right)}\right]$$

($GB/A_{No}^+ = \omega_p^+$)

where GB = Gain BW product = $\frac{g_{mI}}{C_c}$

A_{No}^+ = DC PSRR+ = $\frac{g_{mI} g_{mII}}{G_I g_{ds6}}$

$|p_2| = \frac{g_{mII}}{C_{II}}$ ← output pole

$\omega_p^+ = \frac{GB}{A_{No}^+}$

To maximize PSRR+: (@dc) decrease g_{ds6}, raise g_{mII}

$$PSRR^- = A_{No}^- \left[\frac{\left(1+\frac{s}{GB}\right)\left(1+\frac{s}{|p_2|}\right)}{\left(1+\frac{s}{\omega_p^-}\right)}\right]$$

where $A_{No}^- = \frac{g_{mI} g_{mII}}{G_I g_{ds7}}$

$GB = \frac{g_{mI}}{C_c}$ $\quad \omega_p^- = \frac{G_I}{C_c + C_I} \approx \frac{G_I}{C_c}$

$|p_2| = \frac{g_{mII}}{C_{II}}$

To maximize PSRR−: ① decrease g_{ds7}

② increase $g_{mII} = g_{m6}$

Remarks.

① Since often $g_{ds7} < g_{ds6}$ → often PSRR⁻ > PSRR⁺ (@dc)

② $\frac{\omega_p^-}{\omega_p^+} = \frac{\cancel{g_{m1}}/\cancel{C_c}}{\frac{\cancel{C_1} g_{ds6}}{g_{m1}\cancel{C_c}}} = \frac{g_{m1}}{g_{ds6}}$ → that's quite large

$\therefore \omega_p^- \gg \omega_p^+$

Thus, for an NMOS input op amp, PSRR⁻ is often better than PSRR⁺. → in design, need to worry more about PSRR⁺!

③ Some methods for reducing PSRR:

(i) Use buffer-based zero-cancellation in the compensation loop.

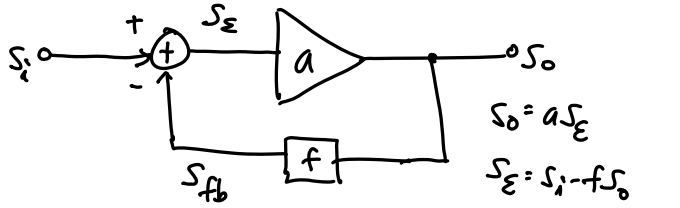
(ii) Use cascode circuitry, or balanced circuit topologies.

(iii) Supply-independent biasing.

(iv) Design strategies to minimize parasitic capacitive feedthrough.

Feedback

⇒ we know this:



$S_o = a S_\varepsilon$

$S_\varepsilon = S_i - f S_o$

⇓

$$\frac{S_o}{S_i} = \frac{a}{1+af} = A$$

Benefits of Negative FB

① Stabilizes the gain of the amp against parameter changes & active device variations

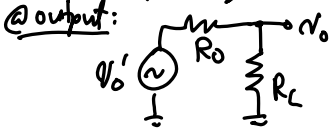
② Modifies R_i and R_o → basically improves their values according to the type of amplifier implemented

e.g., voltage amp: R_i: large, R_o: small

@ input:

If R_i: large, $V_i \approx V_s$. ($R_i \gg R_s$)

@ output:



If R_o: small, $V_o \approx V_o'$. ($R_o \ll R_L$)

current-to-voltage amp: R_i: small, R_o: small

voltage-to-current amp: R_i: large, R_o: large

current-to-current amp: R_i: small, R_o: large

③ Reduces distortion; improves linearity.

④ Increases bandwidth (ω_{-3dB}).

Disadvantages of Neg. FB

① Gain is reduced → reduction factor ~ equal to the amount of gain stabilization, distortion reduction, etc...

Solution: Add more stages of gain → but this adds cost & power...

② Feedback causes stability problems (if not compensated properly)

Gain Sensitivity Reduction via FB

$$A = \frac{a}{1+af} \rightarrow \frac{dA}{da} = \frac{(1+af) - af}{(1+af)^2} = \frac{1}{(1+af)^2}$$

loop gain

For a Δ in op amp gain: δa

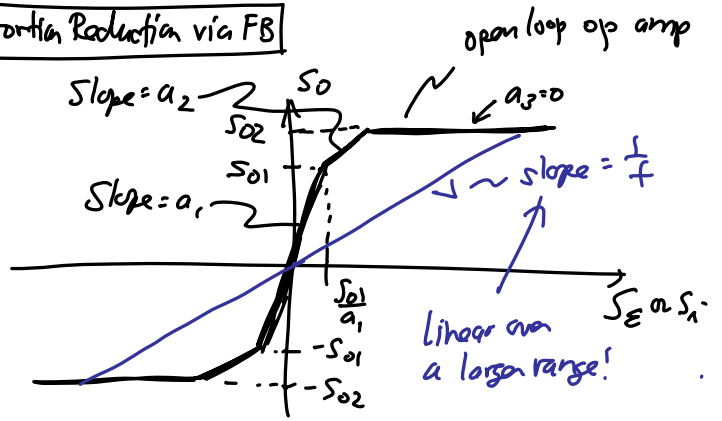
$$\frac{\delta A}{\delta a} = \frac{1}{(1+af)^2} \rightarrow \delta A = \frac{\delta a}{(1+af)^2}$$

much smaller than δa

... and the fractional change:

$$\frac{\delta A}{A} = \frac{1+af}{a} \frac{\delta a}{(1+af)^2} \Rightarrow \boxed{\frac{\frac{\delta A}{A}}{\frac{\delta a}{a}} = \frac{1}{1+af}}$$

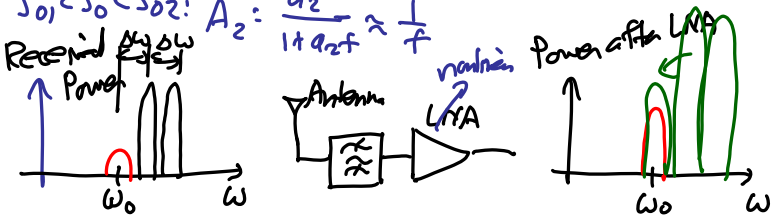
Distortion Reduction via FB



Now, close the loop (using FB):

$0 < S_0 < S_{01}$: $A_1 = \frac{a_1}{1+a_1 f} \approx \frac{1}{f}$ for a_1 large: 20k

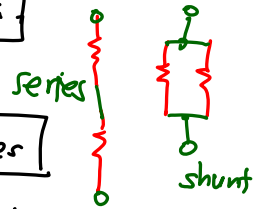
$S_{01} < S_0 < S_{02}$: $A_2 = \frac{a_2}{1+a_2 f} \approx \frac{1}{f}$ maybe $a_2 \sim 100 - 1{,}000$



"Inspection" Analysis of FB Ckts.

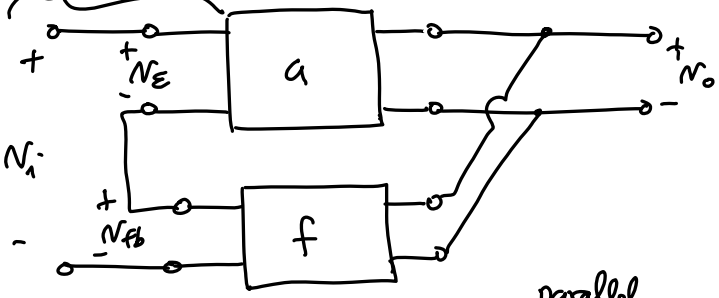
↓ starts with...

Identification of FB Connection Types



Series Connection - FB network part in series w/ amplifier part

↳ must go thru both the FB part & the amplifier part to get from the node of interest to ground



parallel

Shunt Connection - FB network part in shunt w/ amplifier part

↳ can get from the node of interest to ground via either FB network part or the amplifier part

over