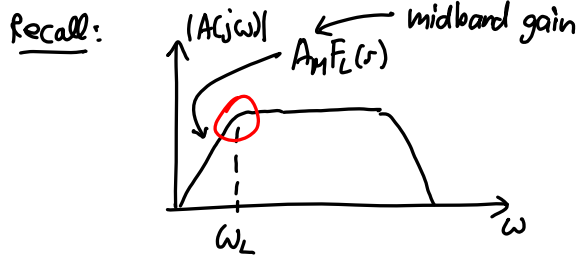


Lecture 7: Active Loads I

- Announcements:
- Lab 1 this week - report to your lab section
- Lecture Topics:
  - ↳ Short Ckt Time Constant (SCTC) Analysis
  - ↳ Example Low Freq. Response Determination
  - ↳ Active Loads
    - Why active loads?
    - Examples of actively loaded amplifiers
- -----
- Last Time:

Low Freq. Amplifier Response Using Short Circuit Time Constant Analysis (SCTC)



In general, for the low freq. response:

$$F_L(s) = \frac{s^{n_z} + d_1 s^{(n_z-1)} + \dots}{s^{n_p} + e_1 s^{(n_p-1)} + \dots}, \quad n_z = \# \text{ poles} = \# \text{ zeros}$$

We can express the coefficient  $e_1$  by:

$$e_1 = \omega_{p1} + \omega_{p2} + \dots + \omega_{pn_z}$$

For the case of a dominant pole:  
↳ i.e., the highest freq. pole

Similar analysis  
to that used  
for OCTC...

$$F_L(s) \cong \frac{s}{s + \omega_L} = \frac{s}{s + e_1} \rightarrow e_1 \cong \omega_{p1} = \omega_L$$

$$\therefore \omega_L \cong e_1 = \sum_j \omega_{pj} = \sum_j \frac{1}{C_j R_{js}} = \sum_j \frac{1}{\tau_{js}}$$

where  $C_j \triangleq$  various large ( $> 10 \text{ nF}$ ) capacitors in the ckt. (e.g., the bypass caps.)

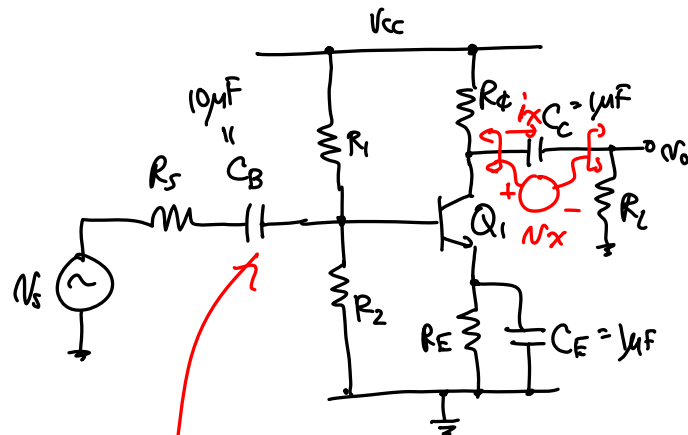
$R_{js} \triangleq$  driving point resistance seen between the terminals of  $C_j$  determined with:  
For readability, can go to Sedra & Smith

- ① all large capacitors short-circuited, except  $C_j$ , which is replaced by the test voltage source for  $R$  determination
- ② all independent sources eliminated (i.e., short voltage sources, open current sources)
- ③ open all H.F. capacitors (i.e., small caps in the pF range, or  $< 1 \text{ nF}$ )

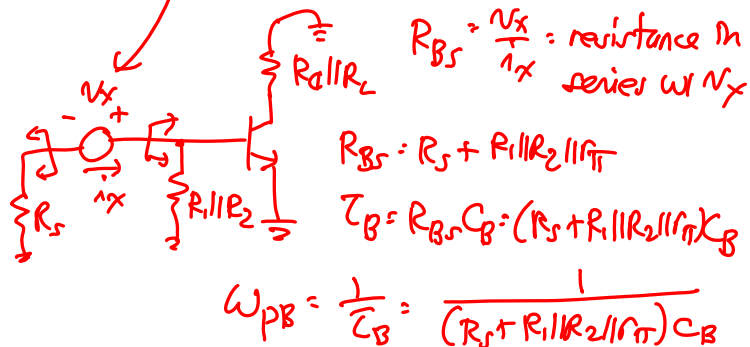
Again, for the case where there are no dominant poles, a reasonable approximation is:

$$\omega_L \cong \sqrt{\omega_{p1}^2 + \omega_{p2}^2 - 2\omega_{z1}^2 - 2\omega_{z2}^2}$$

Ex: Determine the L.F. response of the C.E. Amplifier



(a)  $\tau$  due to  $C_B$ : short  $C_C$  &  $C_E$



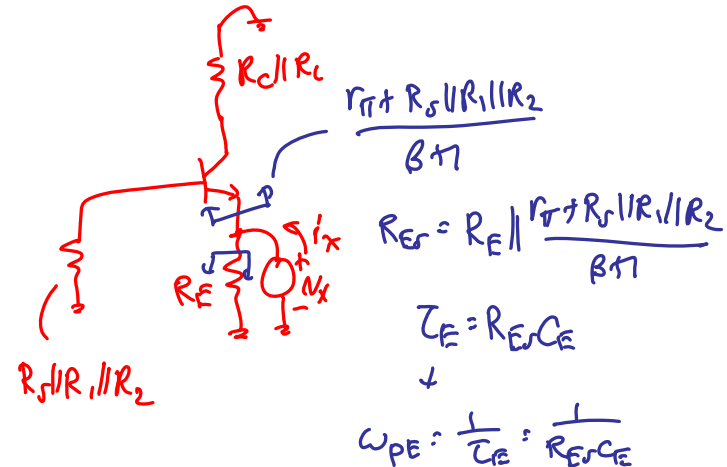
(b)  $\tau$  due to  $C_C$ : short  $C_B$  &  $C_E$

$\Rightarrow$  again  $R_{CS}$ : resistance in series seen on both sides

$$\tau_C = (R_L + r_o || R_C) C_C \rightarrow \omega_{PC} = \frac{1}{\tau_C} = \frac{1}{(R_C || R_L) C_C}$$

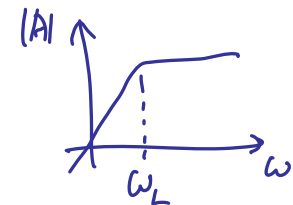
$\uparrow$   
 $R_C$

(c)  $\tau$  due to  $C_E$ : short  $C_B$  &  $C_C$



and finally:

$$\omega_L = \omega_{PB} + \omega_{PC} + \omega_{PE}$$



Active Loads

⇒ Why use them?  $G_{m0} = \frac{N_0}{N_i} = -g_m R_D$

For  $\frac{N_0}{N_i} \uparrow$ , must:

① Raise  $g_m \rightarrow$  raise  $I_D$

Problem:  $V_{R_D} = I_D R_D \uparrow$

Limited by supply  $V_{DD}$

② raise  $R_D \rightarrow$  again,  $V_{R_D} \uparrow$

another problem: area consumption by  $R_D$

Layout:

polySi  $\sim 1k\Omega$

high cost!

beta solution:

Types of Active Loads → current a current source

Diode-Connected Enhancement Load:

Depletion Load:

ancient & we won't consider this

to drive X'sistor

Diode-Connected PMOS Load:

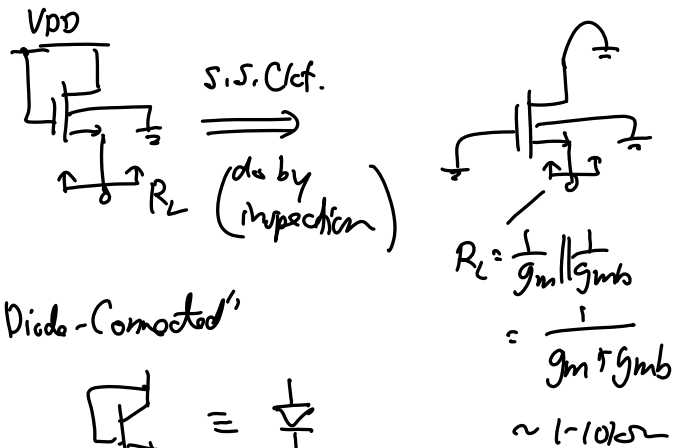
PMOS Current Source Load:

$V_{B1A5}$

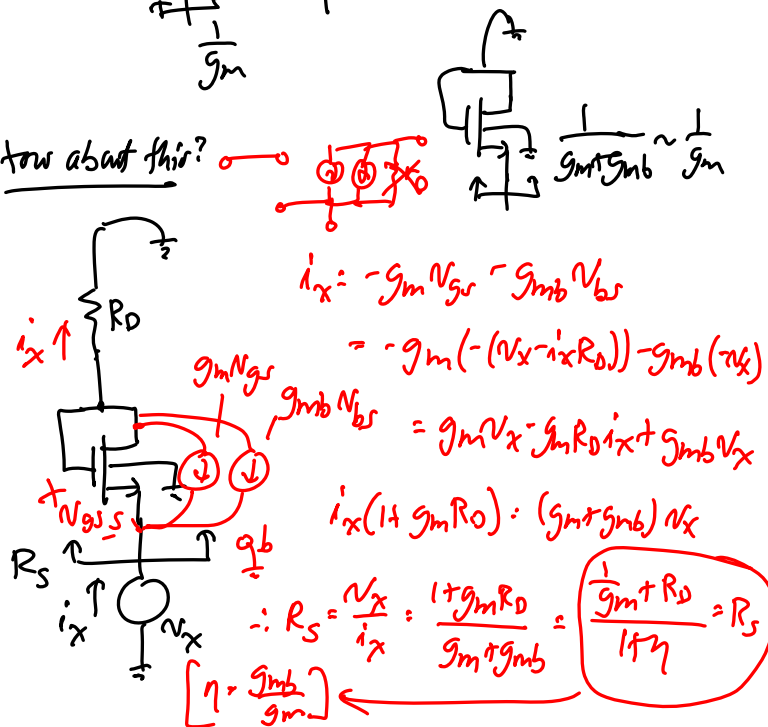
Norton Equivalent:

ideal when  $R_S = \infty$

### Diode-Connected Enhancement Load

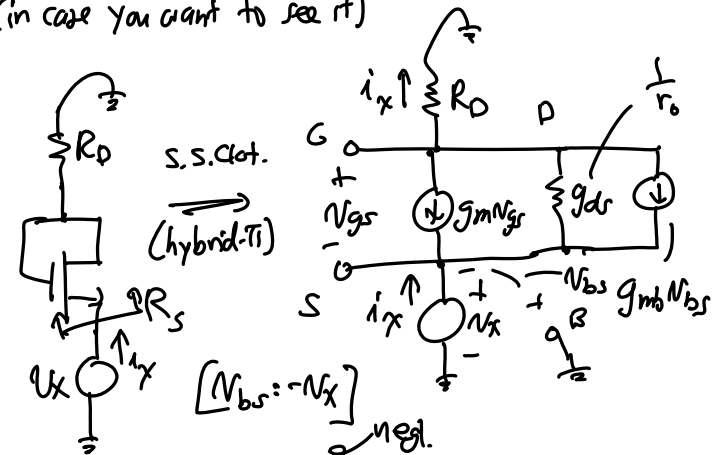


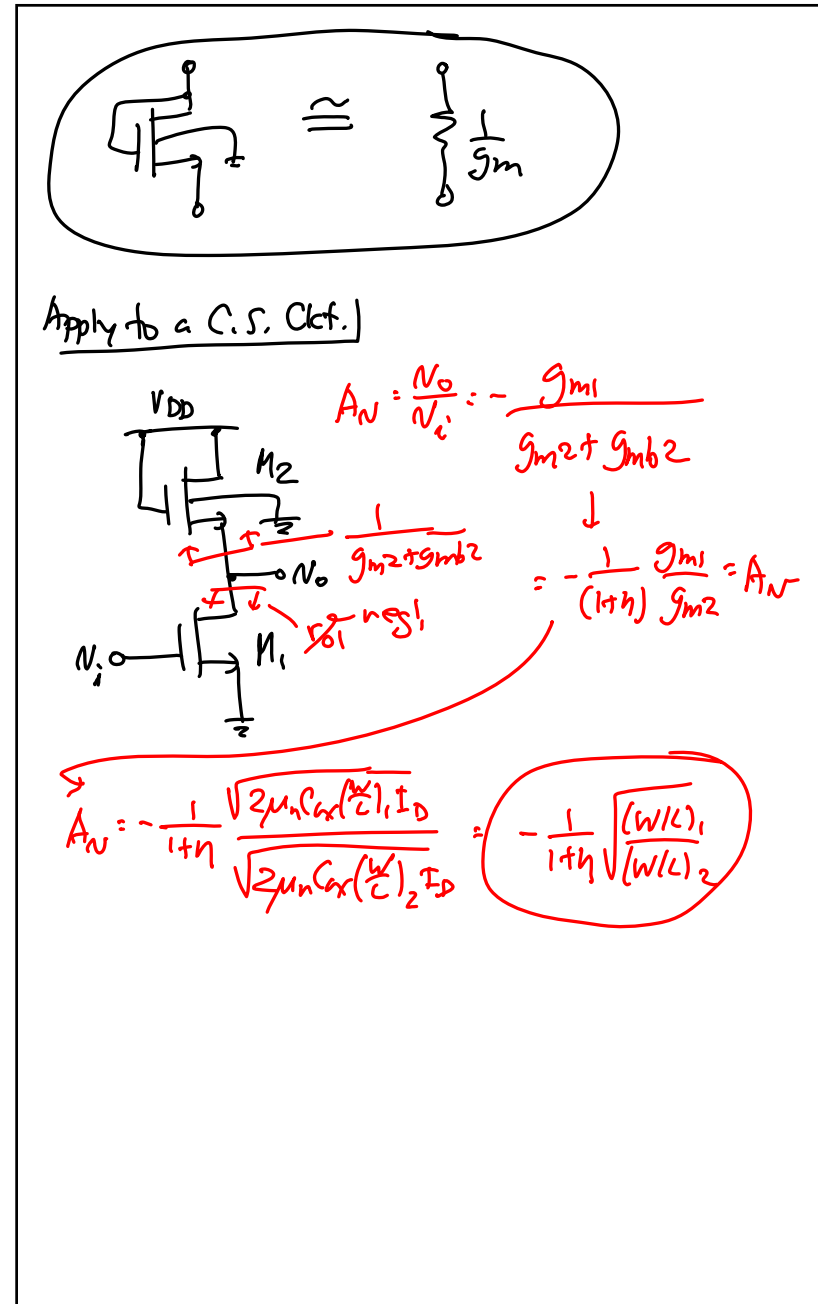
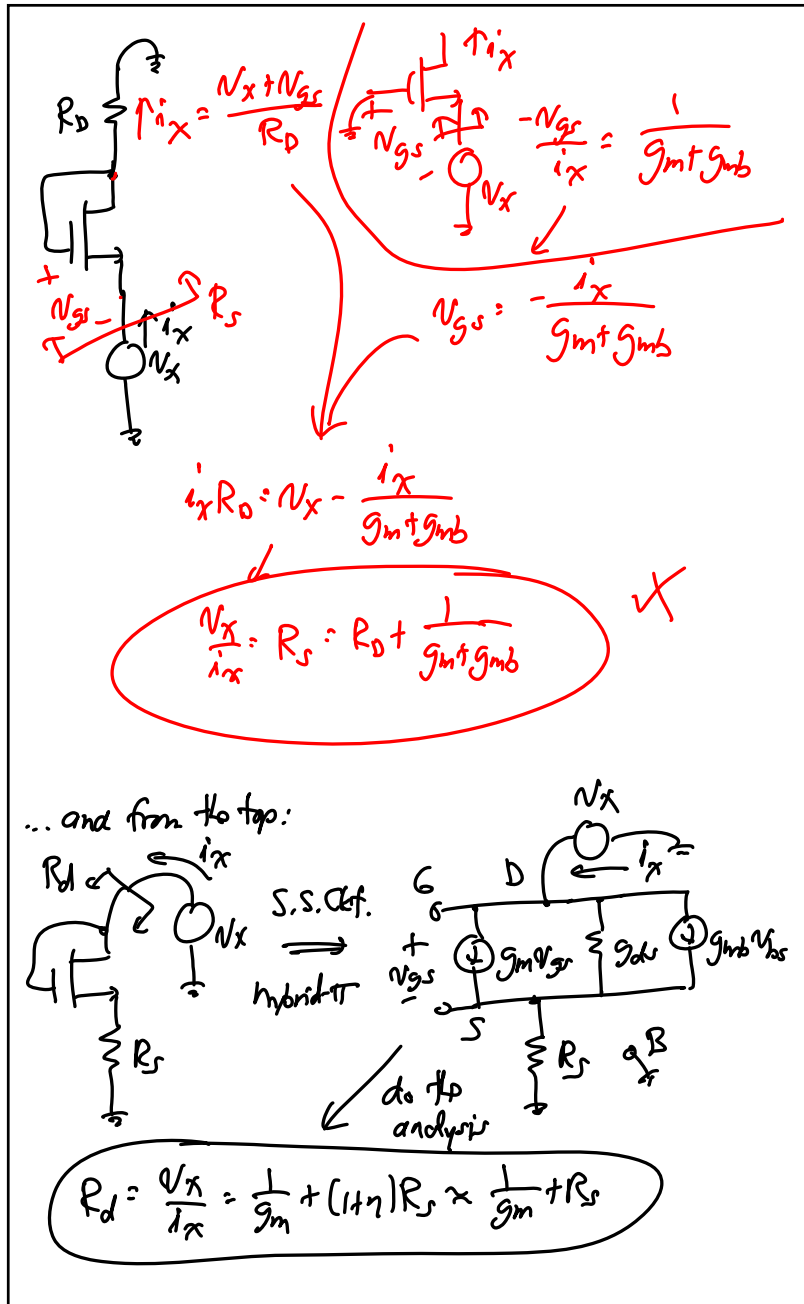
How about this?



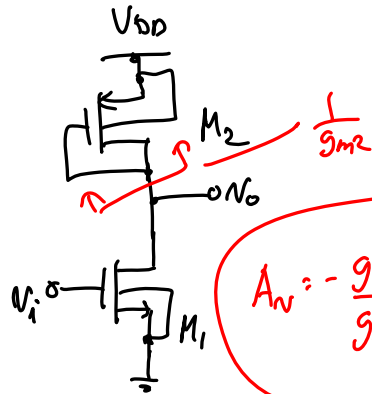
### Full hybrid- $\pi$ analysis:

(in case you want to see it)



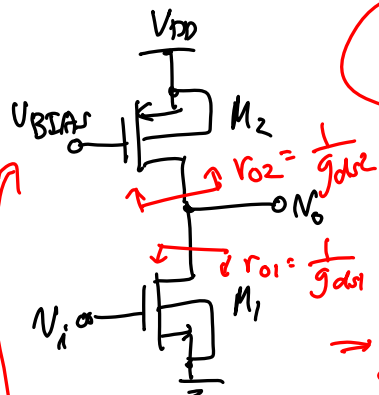


### Diode-Connected PMOS Load



$$A_v = -\frac{g_{m1}}{g_{m2}} = -\frac{\mu_n(W/L)_1}{\mu_p(W/L)_2}$$

### PMOS Current Source Load

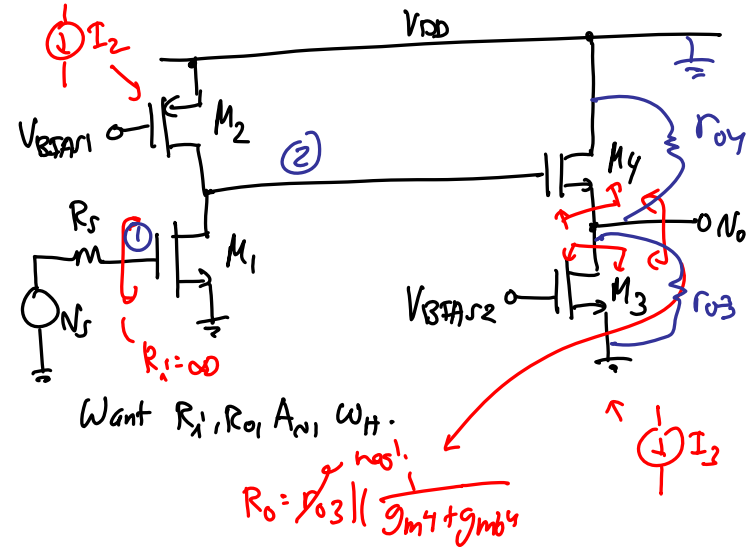


$$A_v = \frac{N_O}{V_i} = -g_{m1}(r_{o1} \parallel r_{o2})$$

$$\approx -\frac{g_{m1}}{g_{ds1} + g_{ds2}}$$

⇒ gain is huge! ( $r_o \approx \text{huge}$ )  
⇒ but requires  $V_{BIAS}$

### Ex. Multi-Stage Actively-Loaded MOS Ckt.

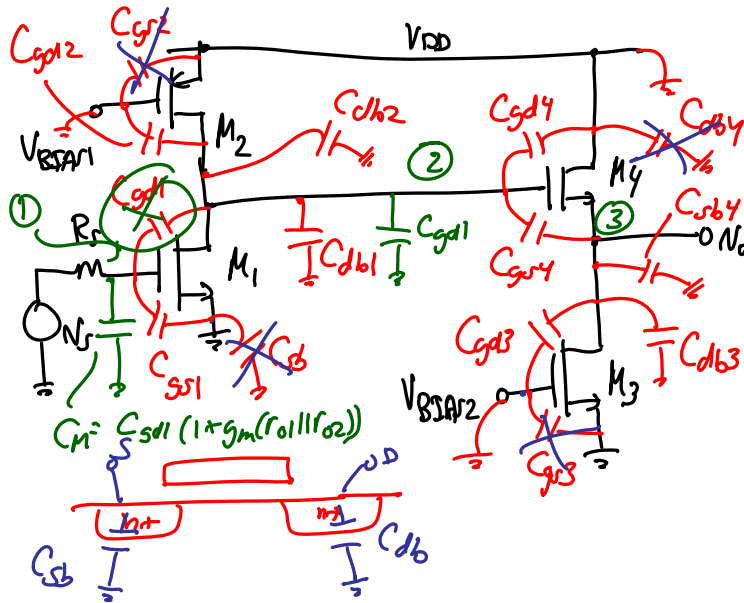


$$A_v = \frac{N_O}{V_i} \cdot \frac{N_O}{V_{B1}} \cdot \frac{N_O}{V_{B2}} \rightarrow$$

$$= (1)(-g_{m1}(r_{o1} \parallel r_{o2})) \cdot \frac{g_{m4}(r_{o3} \parallel r_{o4})}{1/(g_{m4} + g_{mb4})(r_{o3} \parallel r_{o4})}$$

$$A_v = -g_{m1}(r_{o1} \parallel r_{o2}) \left( \frac{g_{m4}}{g_{m4} + g_{mb4}} \right)$$

Now, fiddle freq. response:



$$\tau_1 = [C_{gs1} + C_{gd1}(1 + g_{m1}(r_{o1} || r_{o2}))] R_s$$

$$\tau_2 =$$