Lecture 8: Active Loads II & Current Sources

- **Announcements:**
  - HW#3 due tomorrow at 8 a.m.
  - HW#4 will be online soon
  - Lab tomorrow – go to your lab section
- **Lecture Topics:**
  - Analysis of actively loaded circuits (continued)
  - Current Sources
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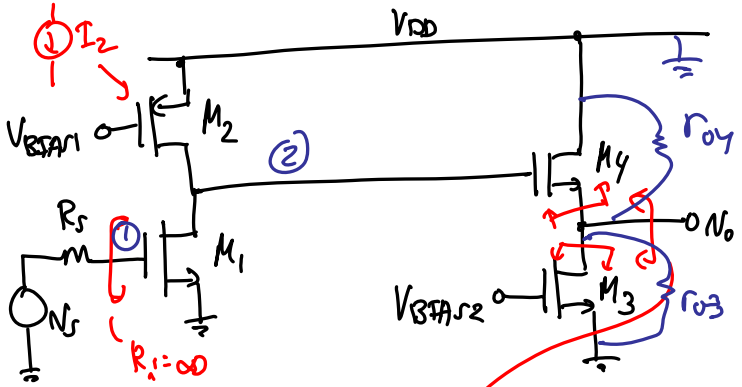
- **Last Time:**

Ex. Multi-Stage Actively-load MOS Clef.



Want R_i, R_{o1}, A_{v1}, ω_H, ..

$R_o = r_{O3} \| \frac{1}{g_{m4}+g_{mb4}}$

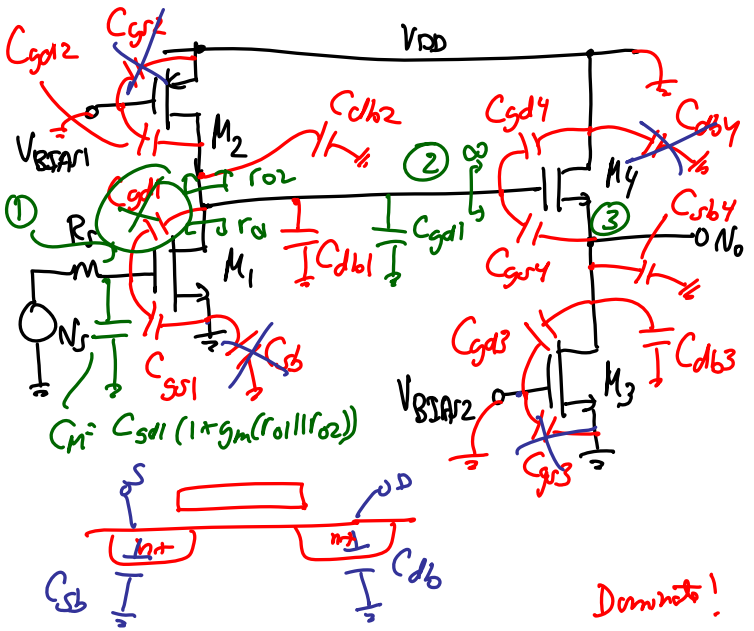
I_3

$a_V = \frac{V_{O1}}{V_S} \cdot \frac{V_{(2)}}{V_{O1}} \cdot \frac{V_O}{V_{(2)}}$

$= (1)(-g_{m1}(r_{O1} \| r_{O2})) \cdot \frac{g_{m4}(r_{O3} \| r_{O4})}{1+(g_{m4}+g_{mb4})(r_{O3} \| r_{O4})}$

$a_V = -g_{m1}(r_{O1} \| r_{O2}) \left(\frac{g_{m4}}{g_{m4}+g_{mb4}}\right)$

Now, to do freq. response:



$C_M = C_{gd1}(1+g_m(r_{O1} \| r_{O2}))$

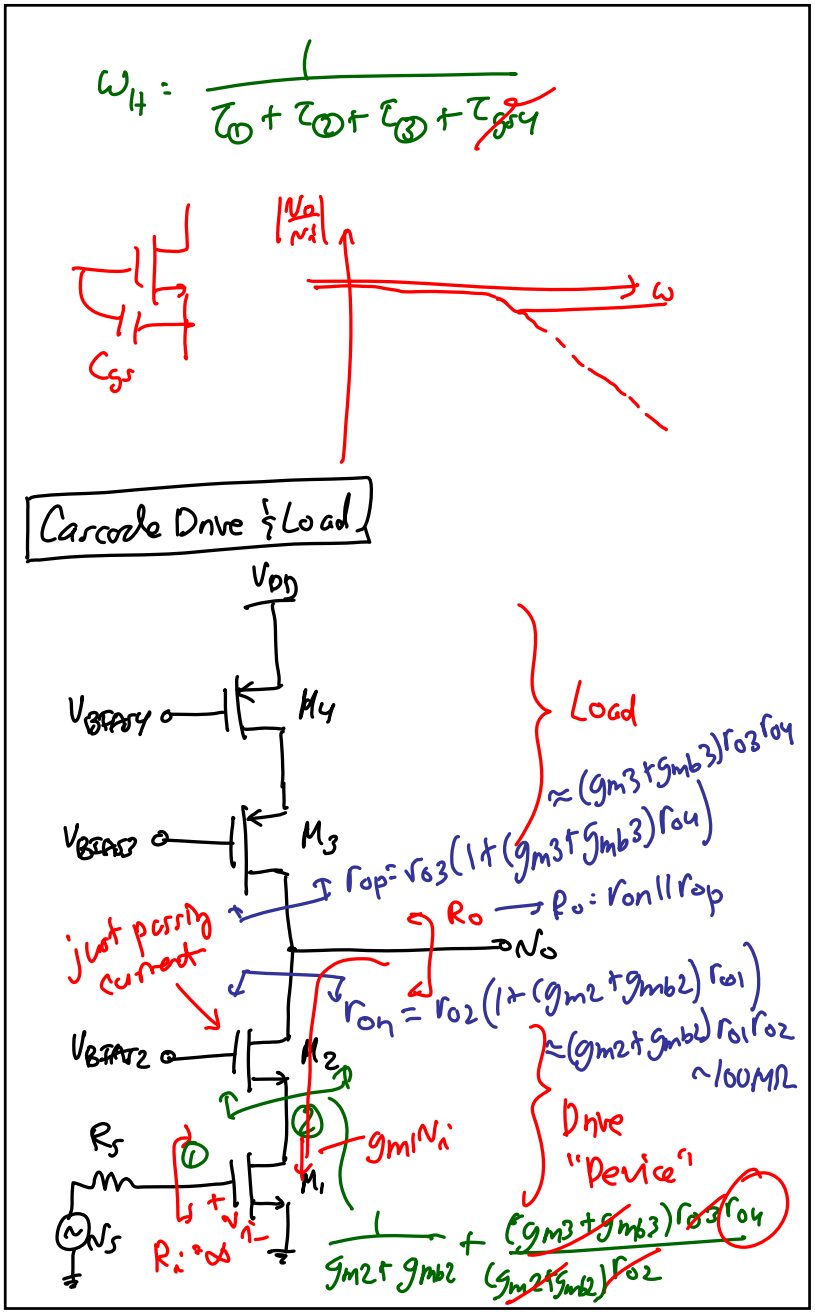
Dominate!

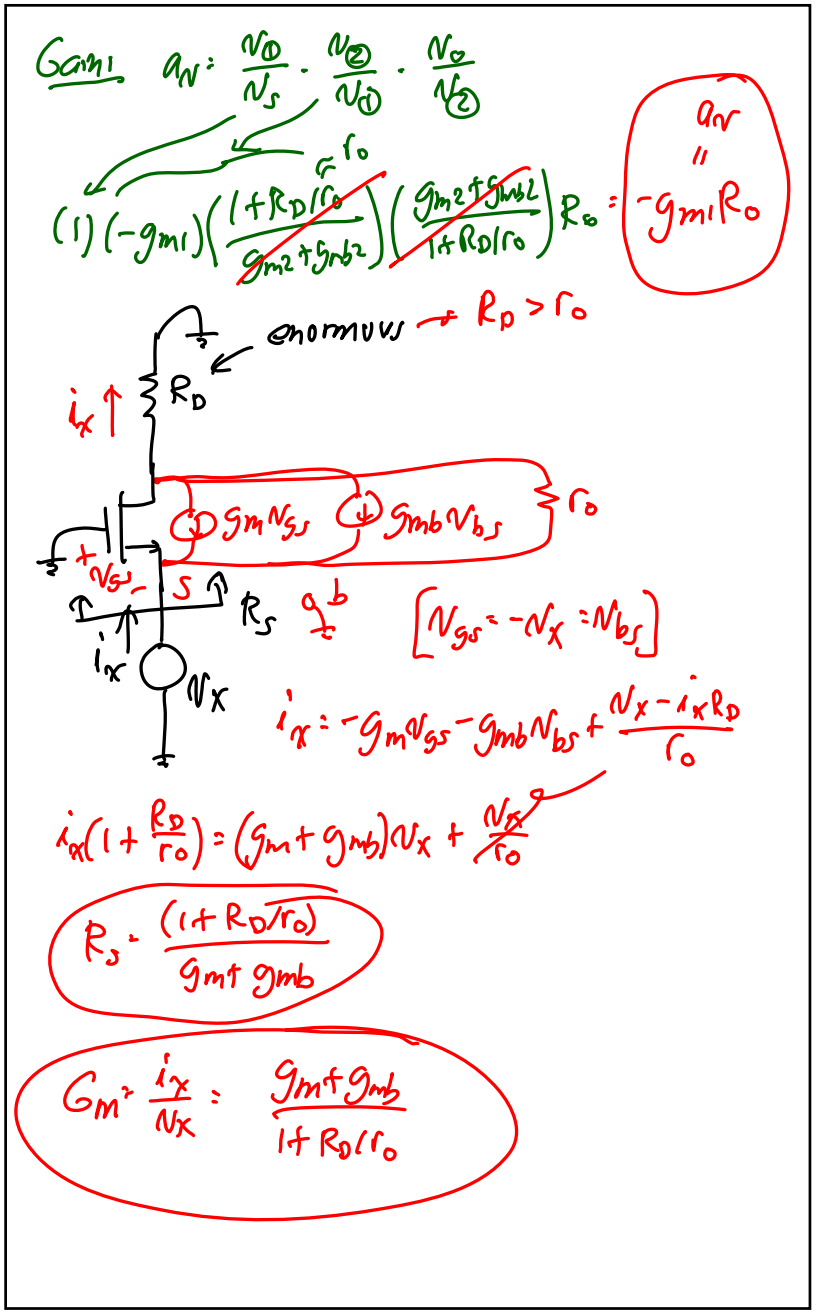
$\tau_{①} = [C_{gs1} + C_{gd1}(1+g_{m1}(r_{O1} \| r_{O2}))] R_S$

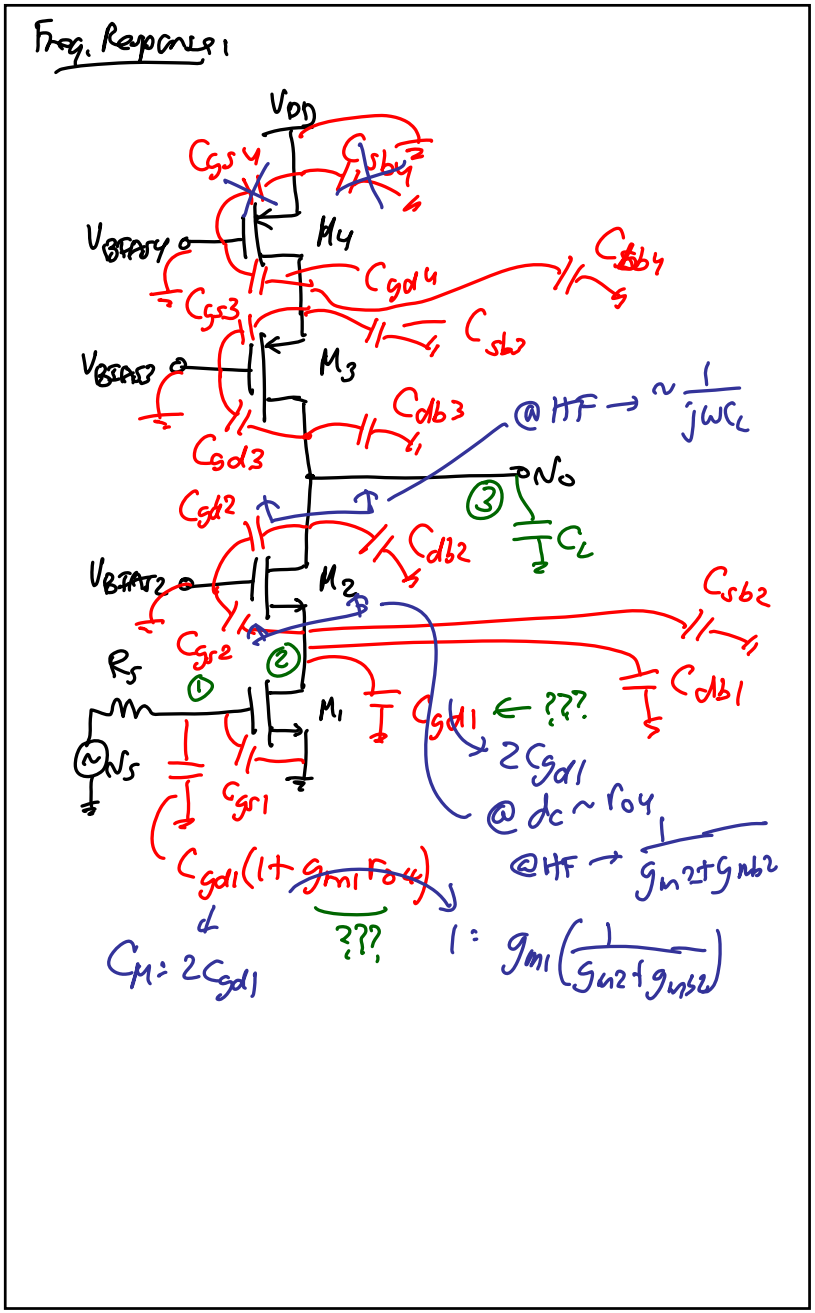
$\tau_{②} = [C_{db1} + C_{gs1} + C_{db2} + C_{gd2} + C_{gd4}](r_{O1} \| r_{O2})$

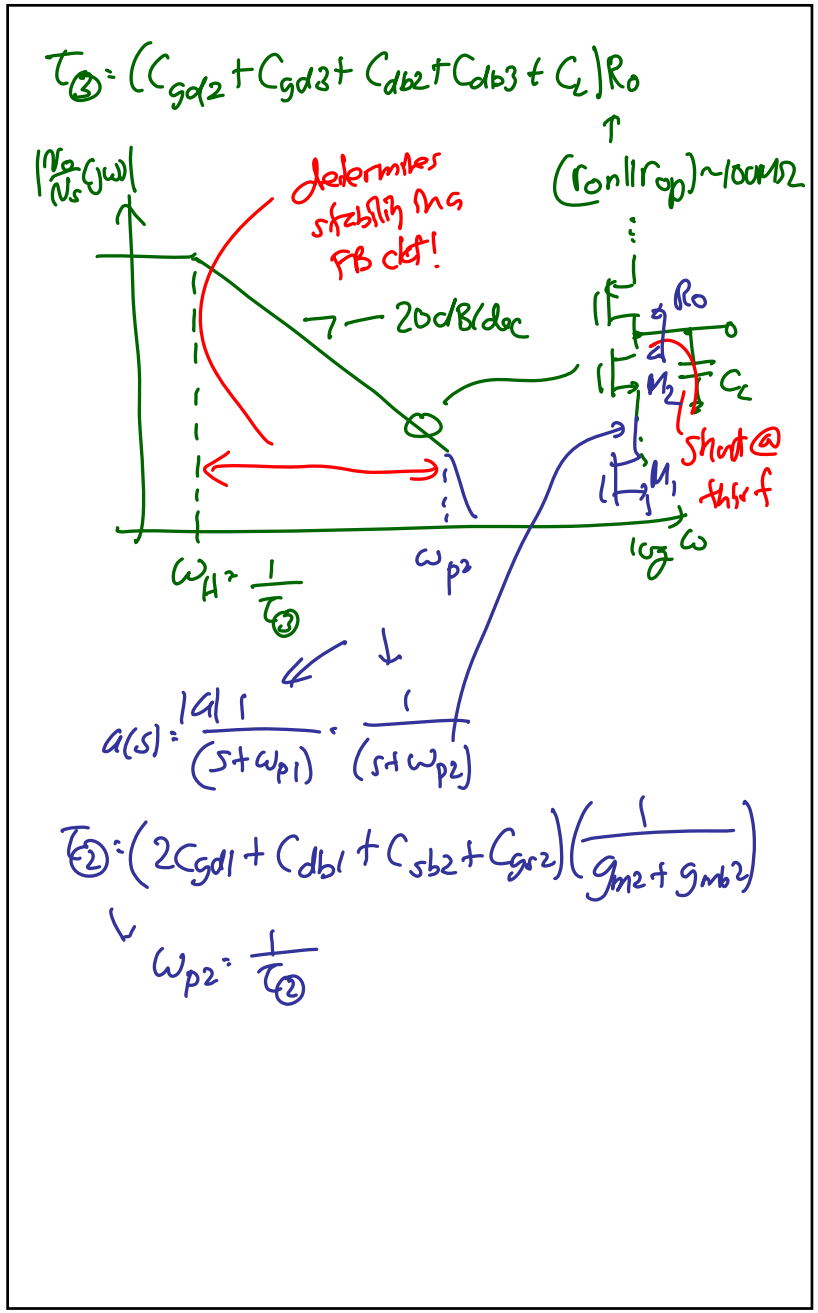
$\tau_{③} = (C_{gd3} + C_{db3} + C_{sb4})\left(\frac{1}{g_{m4}+g_{mb4}}\right)$ ✗

$\tau_{gs4} = C_{gs4}\left[\frac{(r_{O1} \| r_{O2}) + (r_{O3} \| r_{O4}) + 2}{1+(g_{m4}+g_{mb4})(r_{O3} \| r_{O4})}\right]$ ✗


Cascode Drive & Load
Load
Drive "Device"
just passing current
Ri = ∞

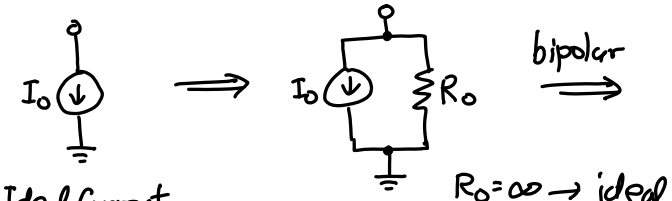

enormous → RD > ro
[Vgs = -Vx : Vbs]





Transistor Current Sources

How can a transistor implement a current source?



Ideal Current Source

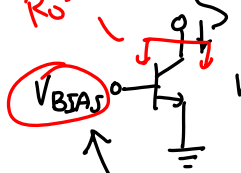
Actual Current Source

Bipolar

Forward-Active Xsistor Current Source

$I_O = I_C = I_S \exp\left(\frac{V_{BIAS}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right)$

$R_O = r_o = \frac{V_A}{I_C}$



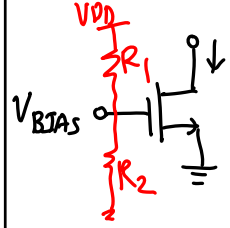
Very stable if V_{BIAS} = const. & V_A = large

Note that V_{BIAS} must be very accurate due to exponential γ to several sig. figs.

↳ e.g., $V_{BIAS} = 0.68745V$

MOS

Saturated MOS Xsistor Current Source



$I_O = I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{BIAS} - V_t)^2(1 + \lambda V_{DS})$

↖ Again, very stable if V_{BIAS} = const. & λ = small

Problem: need to generate a stable V_{BIAS}

We now focus on methods for generating V_{BIAS}.

But how do we get this degree of precision using a transistor ckt?

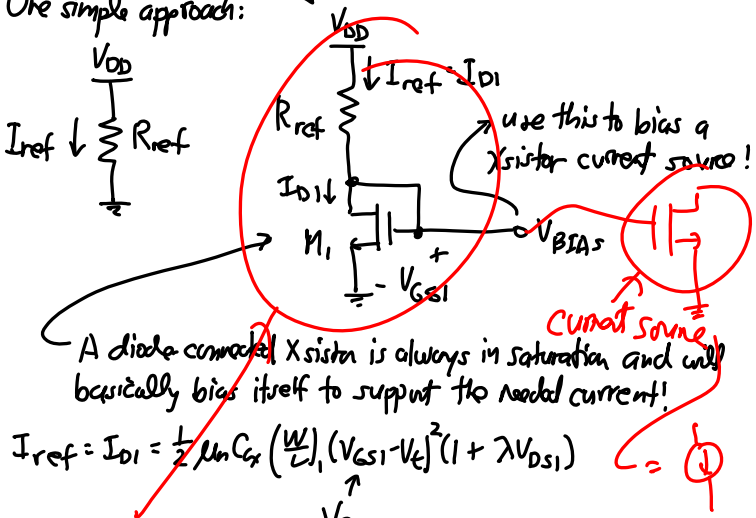
Solution: ↴

Replica Biasing (a simple & effective approach)

1. Generate the desired current.
2. Push the current through a Xsistor and allow it to reach a stable bias pt.
3. Use this stable bias pt. as V_{BIAS}

↳ this can be very precise!

One simple approach:



A diode-connected Xsistor is always in saturation and will basically bias itself to support the needed current!

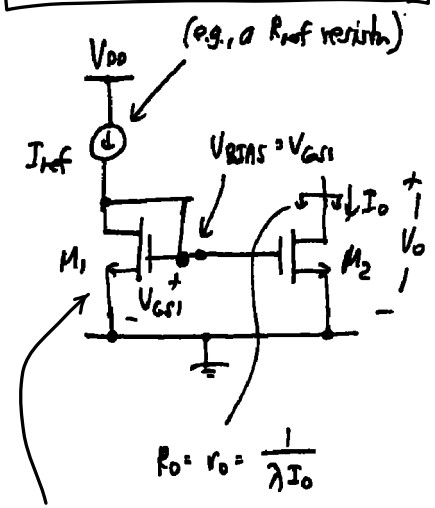
$I_{ref} = I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_t)^2(1 + \lambda V_{DS1})$

V_{BIAS}

↳ Now, can distribute this V_{BIAS} to the gates of many MOS transistor current sources!

V_{BIAS}-Generator

Ex. Simple MOS Current Source



$R_O = r_o = \frac{1}{\lambda I_O}$

Diode-connected Xsistor → saturation:

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{BIAS} - V_t)^2 (1 + \lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{BIAS} - V_t)^2 (1 + \lambda V_{DS2})$$

0.01

In general, $V_{DS1} \neq V_{DS2}$, but if λ = small, then little difference in I_{D1} & I_{D2}

① Case: matched M_1 & M_2 $\Longrightarrow$ $I_O = I_{ref}$

② Case: M_1 & M_2 scaled w/r to each other

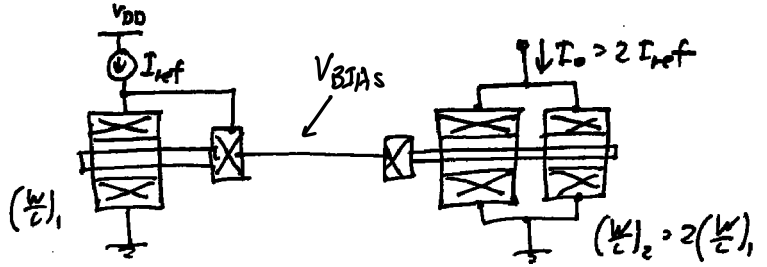
$$\Rightarrow \boxed{I_O = I_{ref}\frac{(W/L)_2}{(W/L)_1}}$$

$\Rightarrow$ use $L_1 = L_2$ for both accuracy, then:

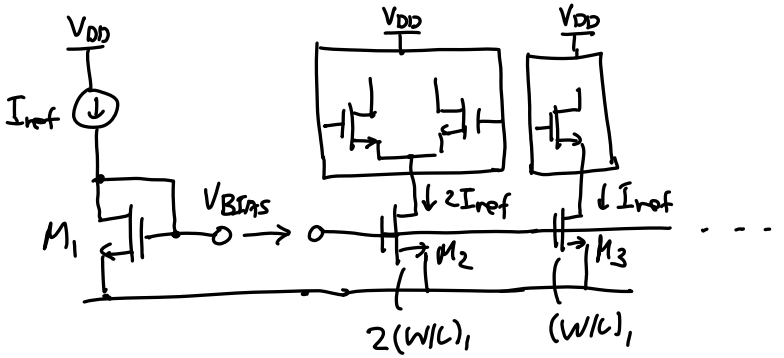
$$\boxed{\frac{I_O}{I_{ref}} = \frac{W_2}{W_1}}$$

Note: For better accuracy, should use multiple copies of one device when scaling currents → reduces edge effects!

Ex: Layout for a Doubling Current Source

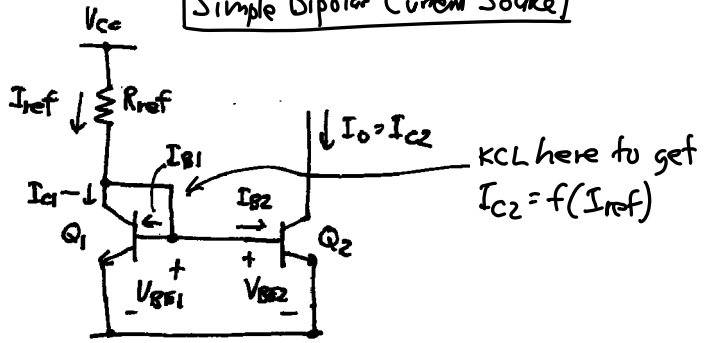


A single V_{BIAS} generator can now serve numerous current sources:



How about bipolar?

Simple Bipolar Current Source



Assume Q_1 & Q_2 are matched. (i.e., $V_A = \infty$)

$V_{BE1} = V_{BE2} \rightarrow I_{C1} = I_{C2} = I_O$ (neglecting V_A's)

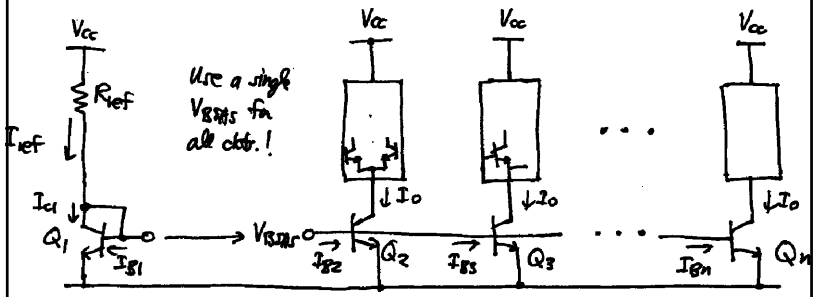
KCL: $I_{ref} = I_{C1} + I_{B1} + I_{B2} = I_{C1}\left(1 + \frac{2}{\beta}\right)$

$\therefore I_{C1} = I_{C2} = I_O = \dfrac{I_{ref}}{1 + \frac{2}{\beta}} \rightarrow I_O \approx I_{ref}$

and $\boxed{I_{ref} = \dfrac{V_{CC} - V_{BE(on)}}{R_{ref}}}$ $\boxed{R_O = r_{O2}}$

can say error $\sim \frac{2}{\beta}$

Again, a single V_{BIAS} generator can serve many current sources throughout the IC chip:



$I_{ref} = I_{C1} + I_{B1} + I_{B2} + I_{B3} + \cdots + I_{Bn}$

[Identical Xistors] $\Rightarrow I_{ref} = I_{C1}\left(1 + \frac{n}{\beta}\right)$

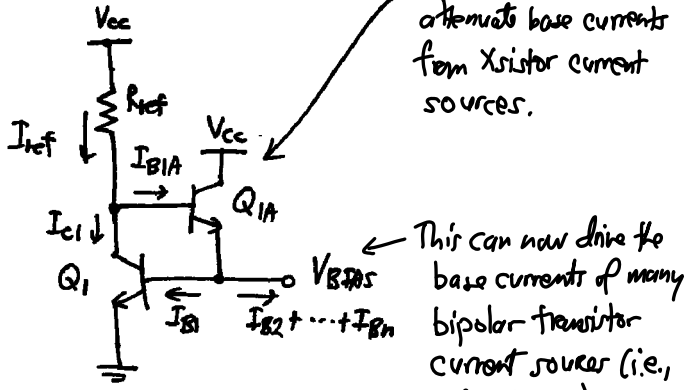
$\Rightarrow \boxed{I_O = I_{C1} = \dfrac{I_{ref}}{\left(1 + \frac{n}{\beta}\right)}}$

Problem: error $\sim \frac{n}{\beta}$ increases as n (I_O deviates from I_{ref}, and the deviation depends on n.)

How can one reduce the error?

To reduce the error term, use a

Buffered V_{BIAS}-Generator



$I_{ref} = I_{C1} + I_{BIA}$

$I_{BIA} = \dfrac{I_{B1} + I_{B2} + \cdots I_{Bn}}{\beta + 1} = \dfrac{n I_{C1}}{\beta(\beta+1)}$

[Assuming identical Xistors]

$I_{ref} = I_{C1}\left(1 + \dfrac{n}{\beta(\beta+1)}\right)$

$\rightarrow \boxed{I_O = I_{C2} = \dfrac{I_{ref}}{1 + \frac{n}{\beta(\beta+1)}} \approx I_{ref}\left(1 - \frac{n}{\beta^2}\right)}$

Note: Now, $\boxed{I_{ref} = \dfrac{V_{CC} - 2V_{BE(on)}}{R_{ref}}}$

Problem: For power savings reasons, oftentimes very small bias currents are needed, on the order of 5μA. This might force too large an R_{ref} in the above bipolar V_{BIAS} generator.