EECS140 Final
Spring 2017

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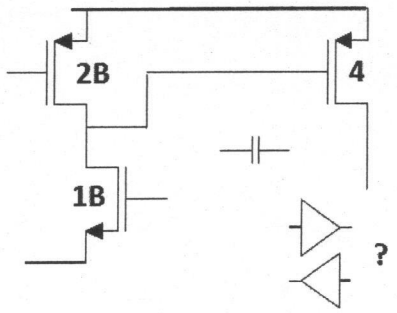
SID _____

Prob.	Score
1,2,3	/24
4,5	/20
6	/18
7,8	/20
9	/22
10, 11	/20
12	/20
13	/12
Total	/156

1. [8] In a vacuum tube, the plate (or anode) current is a function of the plate voltage (output) and the grid voltage (input). $I_P = k(V_P + \mu V_G)^{3/2}$ where μ is a function of the tube geometry.
   a. Calculate $g_m = \frac{\partial I_P}{\partial V_G} = \frac{3}{2} k (V_P + \mu V_G)^{1/2} \mu$ +1 +1
   b. Calculate $g_o = 1/r_o$ $= \frac{\partial I_P}{\partial V_P} = \frac{3}{2} k (V_P + \mu V_G)^{1/2}$
   c. Calculate the intrinsic gain from parts a and b
   $-g_m/g_o = -\mu$ +1 +1 missing minus ok
   d. Can you find intrinsic gain more easily by examining the equation for current? Explain.
   ↳ $I_P = \text{const} \Rightarrow V_P + \mu V_G = \text{const} \Rightarrow \frac{V_P}{V_G} = -\mu$

2. [6] Your friend has designed a two stage Miller compensated op-amp, and is using a unity gain buffer in series with the compensation capacitor. He can't remember if it is supposed to point left or right, or which side of the capacitor it's supposed to be on.
   a. Why use the buffer at all? What is its purpose?
   prevent feedforward current easily RHP zero
   +1 +1
   b. Does it point left or right? Why?
   Left. Provide feedback, not forward
   +1 +1
   c. Which side of the capacitor should it be on? Why?
   Right. Stage 1 needs to see a capacitor to V_{out}



3. [10] You are designing a single-stage CMOS op-amp to be used in feedback to achieve a gain of 50. The gain must be accurate to 1% from DC to 20 Mrad/s. The load is a 1pF capacitor. You are restricted to biasing your transistors with overdrives between 100mV and 1V, and they look reasonably quadratic in that range.
   a. What is the minimum open-loop gain and dominant pole location of the op-amp?
   $f = \frac{1}{50}$ $\frac{1}{Af} < 1\%$ $A > \frac{50}{1\%} = 5K$ ~~$\omega_p = (5K)$~~ $\omega_p \geq 20\,\text{Mrad/s}$
   b. What is the minimum unity gain frequency of the op-amp?
   $(5K)(20\,\text{Mrad/s}) = 100\,\text{Grad/s}$
   c. What is the minimum transconductance of the input transistors?
   $g_m \geq \omega_u C_L = (10^{11}\,\text{rad/s})(10^{-12}\,\text{F}) = 0.1\,\text{S}$
   d. What is the minimum current in each of the input transistors?
   $I_D = \frac{g_m V_{ov}}{2} = \frac{(0.1)(0.1)}{2} = 5\,\text{mV}$

4. [10] An NMOS-input common source amplifier with a PMOS load is biased so that the NMOS transconductance is ten times greater than the PMOS transconductance.
   a. What is the ratio of the PMOS gate noise power, $\bar{v}^2_{n,P}$, to the NMOS gate noise power, $\bar{v}^2_{n,N}$?

   $\overline{v_n}^2 \sim \frac{1}{g_m}$ $\quad \frac{\overline{v_{n,P}}^2}{\overline{v_{n,n}}^2} = \frac{g_{mn}}{g_{mp}} = 10$

   b. What is the ratio of the gain from the PMOS gate to the output, A_{VP}, to the gain from the NMOS gate to the output, A_{VN}?

   $A_v \sim g_m$ $\quad \frac{A_{v,P}}{A_{v,n}} = \frac{1}{10}$

   c. What is the total noise power spectral density in Volts squared per Hz at the output, in terms of $\bar{v}_{n,P}$, , A_{VP}, $\bar{v}_{n,N}$, and A_{VN}?

   $\overline{v}^2_{n,P} A^2_{VP} + \overline{v}^2_{n,n} A^2_{Vn}$

   d. What is the total noise power spectral density in Volts squared per Hz at the output in terms of just $\bar{v}_{n,N}$, and A_{VN}?

   $(10\,\overline{v}^2_{n,n})\left(\frac{1}{10} A_{v,n}\right)^2 + \overline{v}^2_{n,n} A^2_{v,n} = 1.1\,\overline{v}^2_{n,n} A^2_{v,n}$

   e. What is the total noise power spectral density in Volts squared per Hz at the **input** in terms of just $\bar{v}_{n,N}$, and A_{VN}?

   $1.1\,\overline{v}^2_{n,n}$

5. [10] With the following selection of op-amp topologies, and assuming V_{TN}=-V_{TP}=1V, V_{DD}=5V
   1. NMOS input diff pair with current mirror load
   2. PMOS input diff pair with current mirror load
   3. NMOS input 2 stage Miller compensated
   4. PMOS input 2 stage Miller compensated
   5. NMOS input folded cascode
   6. PMOS input folded cascode

   List which op-amps will work with which applications. If none, write none.
   a) Switched capacitor amplifier with one input grounded -1 none

   6

   b) Unity gain buffer from 0 to 5V

   none

   c) Comparator making comparisons near V_{DD}

   3, 5 or none or 5

   d) Unity gain buffer for signals near mid-rail, with capacitive load

   all

   e) Non-inverting amplifier with gain of 10 driving a 1kΩ resistive load

   4 or none

6. [18] The figure below is a current mirror op-amp. Assuming a 0 to 5V supply, $V_{TN}=-V_{TP}=1V$, and all transistors with the same number are the same size, and that $g_m r_o >> 1$ for all combinations.

a. What is the gain from a differential input (across the gates of 1AB) to the voltage between the gates of 2AB? $-\frac{g_{m1}}{g_{m2}}$ $\frac{g_m}{g_m} = "1"$ -1

b. What is the gain from the gate of 4A to the gate of 5A? $-\frac{g_{m4}}{g_{m5}}$

c. If a differential input causes a differential current i_d in 1A and $-i_d$ in 1B, what is the current at the output if the output is held at small signal ground (e.g., in a G_m calculation)? $*2\ \frac{g_{m4}}{g_{m2}} i_d$ $2\ i_d$ -1 $i_d - 2$

d. What is the low frequency voltage gain? $\frac{g_{m4}}{g_{m2}}\ g_{m1}(r_{o4} \| r_{o5})$ missing $\frac{g_{m4}}{g_{m2}}$ -1

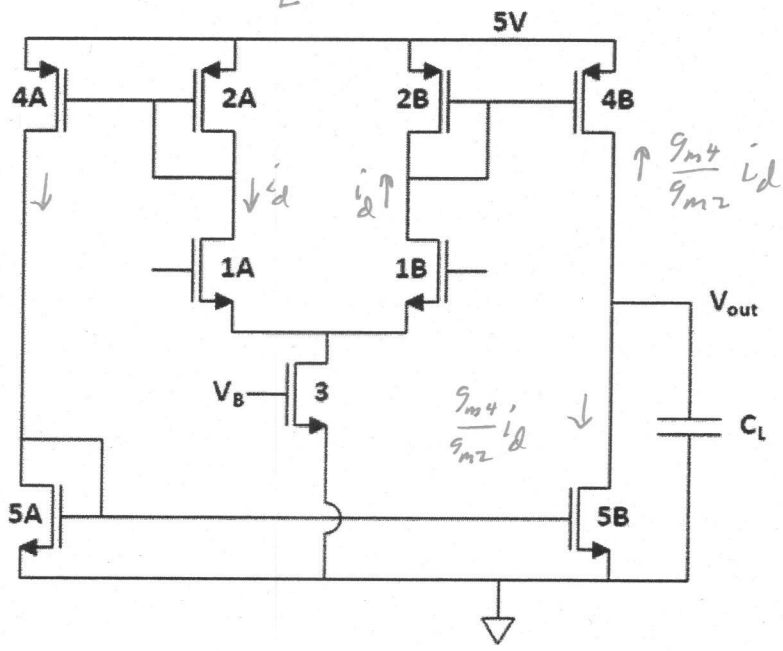
e. What is the input common mode range (min and max)?
min $= V_{TN} + V_{OV3} + V_{OV1}$
max $= V_{DD} - |V_{TP}| + V_{TN} - |V_{OV2}| = V_{DD} - |V_{OV2}|$

f. What is the output swing (min and max)? $[V_{OV5},\ V_{DD} - V_{OV4}]$

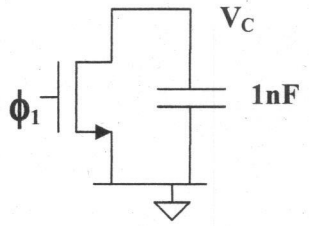
g. What is the frequency of the dominant pole? $\omega_{pout} = \frac{1}{(r_{o4} \| r_{o5}) C_L}$

h. Considering only C_{gs}, what is the frequency response of G_m? (i.e. where are the other poles and zeros?)
$-G_m = \frac{g_{m1}}{2} \frac{g_{m4}}{g_{m2}} \left(\frac{1}{1+s/\omega_{pm2}}\right)\left[1 + \frac{1}{1+s/\omega_{pm5}}\right]$ turns into a doublet $2\left(\frac{1+s/(2\omega_{pm5})}{1+\frac{s}{\omega_{pm5}}}\right)$
$\omega_{pm2} = \frac{g_{m2}}{C_{gs2}+C_{gs4}}$ $\omega_{pm5} = \frac{g_{m5}}{2C_{gs5}}$

i. If you were not happy with the phase margin of this op-amp in unity gain feedback, where would you add capacitance? At C_L



7. [8] The transistor below has V_{TN}=1V, C_{gs}=5pF, C_{gd}=1pF, R_{ON}=1kΩ,



a. If the clock is high, how long does it take for V_C to settle from 100mV to 100μV?

[2] $\tau = RC = 10^3 10^{-9} = 1\mu s$ -1 other than 7τ

[2] $0.1\% \Rightarrow 7\tau = 7\mu s$

b. If the clock goes low (relatively slowly) when V_C has settled to 10mV, what is the impact on V_C during that transition? Give an explanation and a number in Volts.

[2] transistor turns off at $\phi_1 = V_{tn} = 1V$ $\Delta V = + \frac{Q_i}{1nF} = \mp 1mV$ [2]

$Q_i = -V_{tn} C_{gd} = (1V)(1pF) = -1pC$

8. [12] In the switched capacitor circuit below (bookkeep charge)

[1] a. What is the voltage on V- during ϕ_1? 0

b. What is the charge on the right side of C_A and C_B during ϕ_1?

$Q_{AR,1} = -V_{inA} C_A$ $Q_{BR,1} = 0$

all sign errors total -1

[1] c. What is the voltage on V- during ϕ_2? 0

d. What is the charge on the right side of C_A and C_B during ϕ_2?

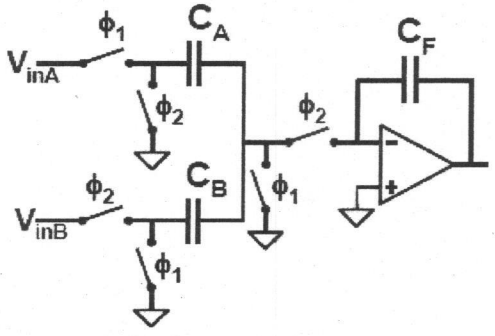
$Q_{AR,2} = 0$ $Q_{BR,2} = -V_{inB} C_B$

e. Where does the charge difference between parts b and d go?

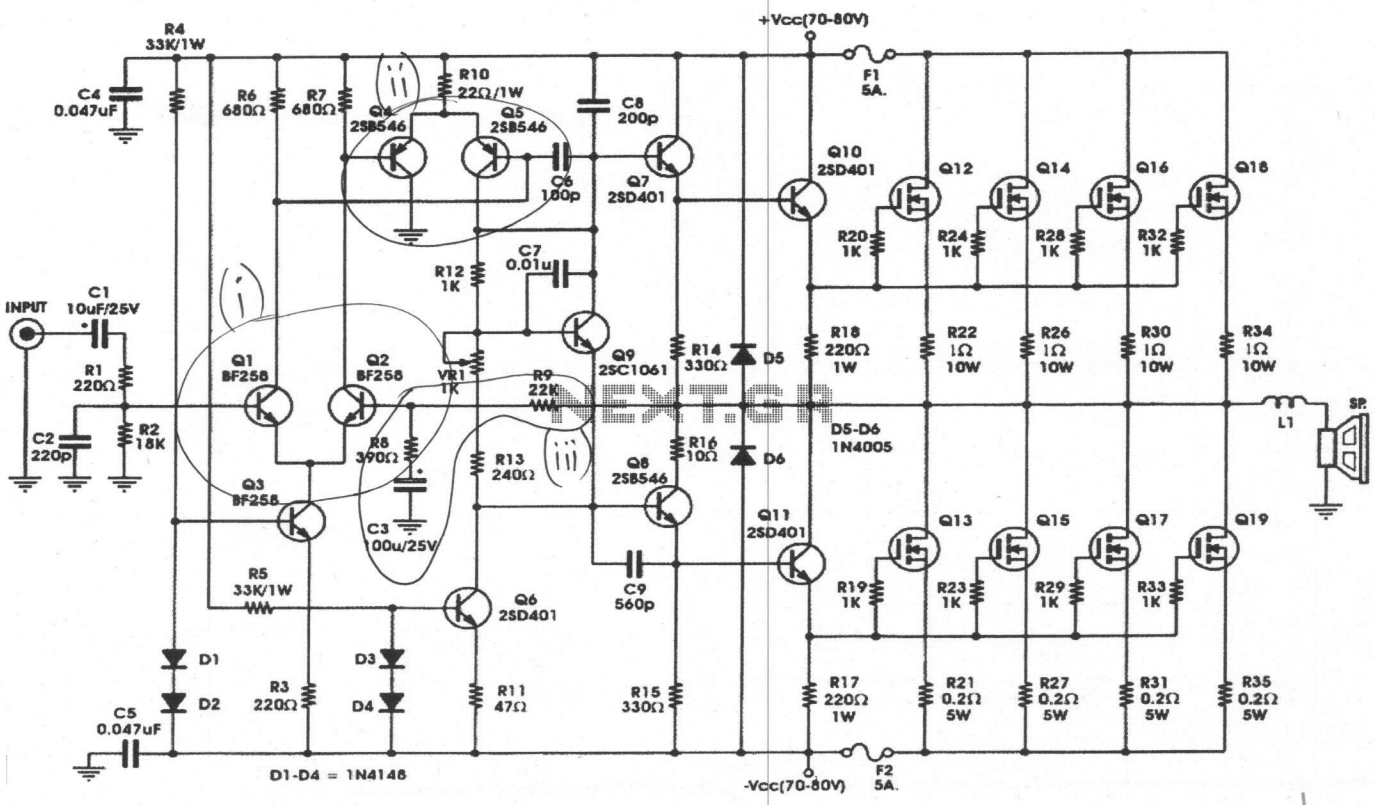
to the left plate of C_F

[4] f. What is the change in V_{out} during one cycle of both clocks?

$\Delta Q_{ABR} = -V_{inA} C_A + V_{inB} C_B$ $V_{out} = 0 + \frac{-\Delta Q_{ABR}}{C_F} = \frac{V_{inA} C_A - V_{inB} C_B}{C_F}$



(Cypress Semiconductor PSoC Application Note)



(http://championed.info/circuit-diagram/audio-amplifier-circuit-diagram.html)

2 pts each

9. [22] In the audio amplifier above, ignore the very weird output stage driving the speaker, and
   a. Circle and label the
      i. input diff pair
      ii. 2nd stage diff pair
      iii. feedback network from the output to V-
   b. Roughly what is the voltage on R3?

      0.7 V

   c. Roughly what is the current through R3? $\frac{0.7V}{220\Omega} \approx 3mA$

   d. Roughly what is the g_m of Q1? $g_m = \frac{I_C}{V_T} = \frac{1.5mA}{26mV} \approx 50mS$

   e. Roughly what is the differential gain of the 1st stage

      $A_{V1} = g_m r_o = (50mS)(680\Omega) \approx 35\ V/V$

   f. Roughly what is the differential to single-ended gain of the 2nd stage?

      $A_{V2} = \frac{g_{m5} r_{o5}}{2}$

   g. What is the DC feedback factor?

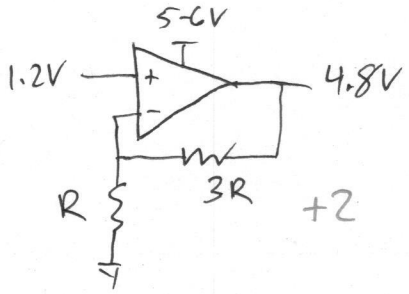
      $f = 1$

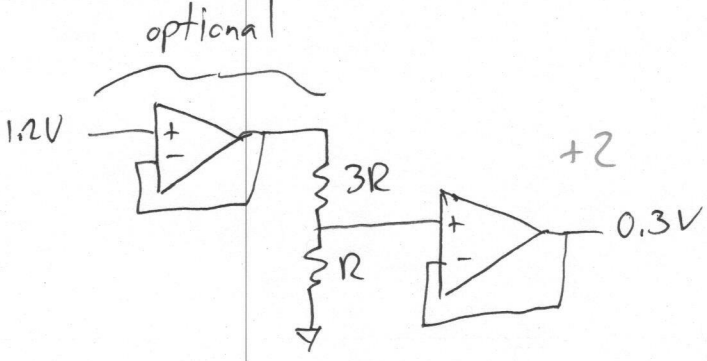
   h. What is the audio-frequency feedback factor? $\frac{R8}{R8+R9}$

   i. What RC time constant determines the lower end of the audio frequency range in the feedback network, and what is that frequency?

      $R8 \cdot C3$ $\quad \frac{1}{400\Omega \cdot 100uF} \approx 25\ rad/s$

10. [12] You have a bandgap that provides a stable 1.2V reference, and a 5 to 6V supply. For other analog components in a system, you need buffered reference voltages of 0.3V and 4.8 V. There is very little current load on those reference voltages. Sketch the op-amp circuits that you would use to generate these voltages, and then draw the schematic of the amplifiers. Be careful of input and output voltages! You may assume that internal op-amp bias voltages are generated elsewhere.





+1 - Low V_{CM} → PMOS input

+1 - Resistive feedback → Must be 2 stages

+1 - High output → Cascodes must be high swing

+1 - Low V_{CM} → PMOS

+1 - Must reach within 300mV of ground

+3 for correct amp schematics

2 pts each

11. [8] The curves below were taken from an N-type FET made at Berkeley with a single carbon nanotube gate and a single molecule of semiconductor, MoS_2 for the body and source/drain. Amazing!

("MoS2 transistors with 1-nanometer gate lengths", Science, October 2016)

a. This N-type device has a negative threshold voltage. Roughly what is it?

-2 V [-2.5 -2]

b. If the width of the device is 1 um, roughly what is the transconductance when VGS=-1V and VDS=2.5V?

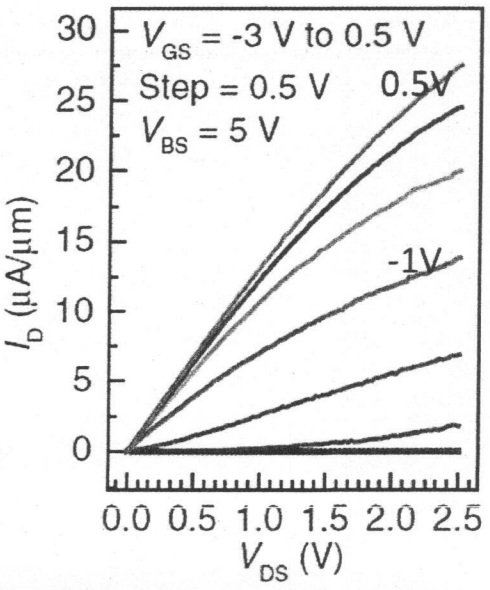
$\frac{5\text{uA}}{0.5\text{V}} = 10^{-5}\,\text{S}$ [10uS 15uS]

c. Roughly what is the output resistance at the same bias point?

$\frac{1.5\text{V}}{6\text{uA}} = 250\text{k}\Omega$ [150kΩ 350kΩ]

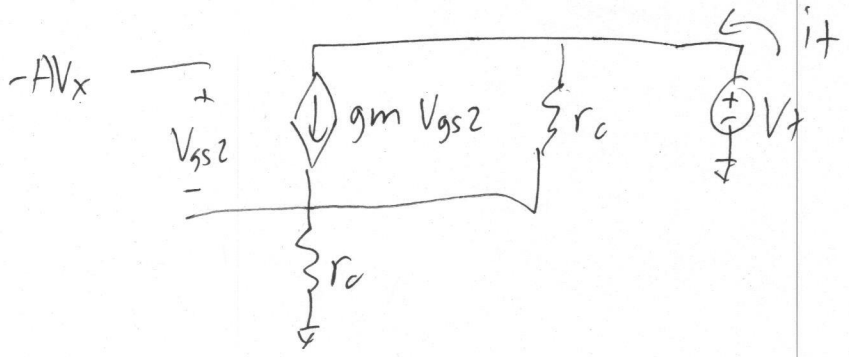
d. What is the intrinsic gain at this bias point?

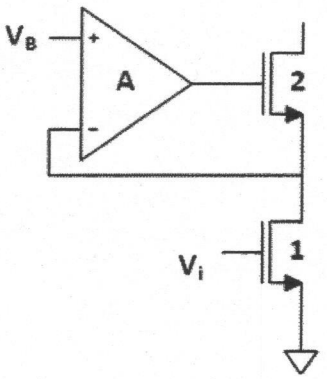
-2.5 V/V



12. [20] For the "gain boosting" sub-circuit in the figure to the below, assuming that the output is at the drain of M2 (load impedance not shown) and that $g_m r_o >> 1$.

4 a. Draw the DC small signal model appropriate for a calculation of R_o.

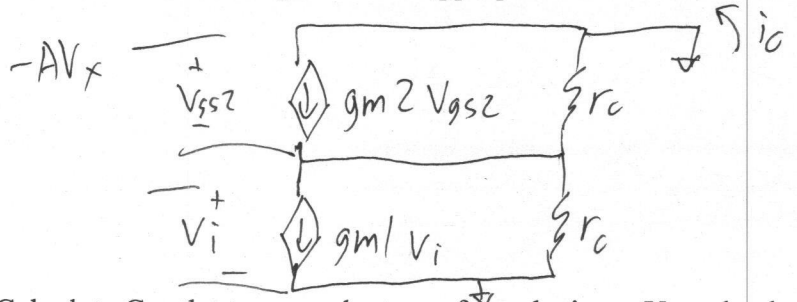




2 b. Calculate R_o, the output resistance seen looking into the drain of M2

$R_o = V_+ / i_+ \cong g_m r_o^2 A$

4 c. Draw the DC small signal model appropriate for a calculation of G_m

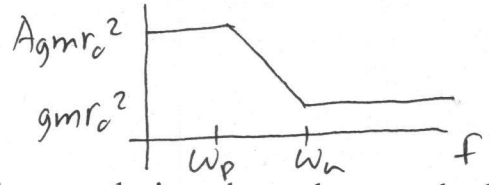


2 d. Calculate G_m, the transconductance from the input V_i to the drain of M2

$G_m \cong g_{m1}$

2 e. If the load impedance were a mirror image made with PMOS devices, how would the gain compare to a similar cascode amplifier without the op-amps? Increases by A times

2 f. If the op-amp gain has a single pole ω_{pA}, sketch the impedance looking into the drain of M2 vs. frequency ignoring all other poles, zeros, caps, etc.



2 g. Compare the impedance above to a load capacitor. Under what conditions will the op-amp frequency response not have a substantial impact on the bandwidth of the overall amplifier?

Pole from $R_o C_L$ should be less than ω_{pA}

2 h. What op-amps would be appropriate from the list in problem 5?

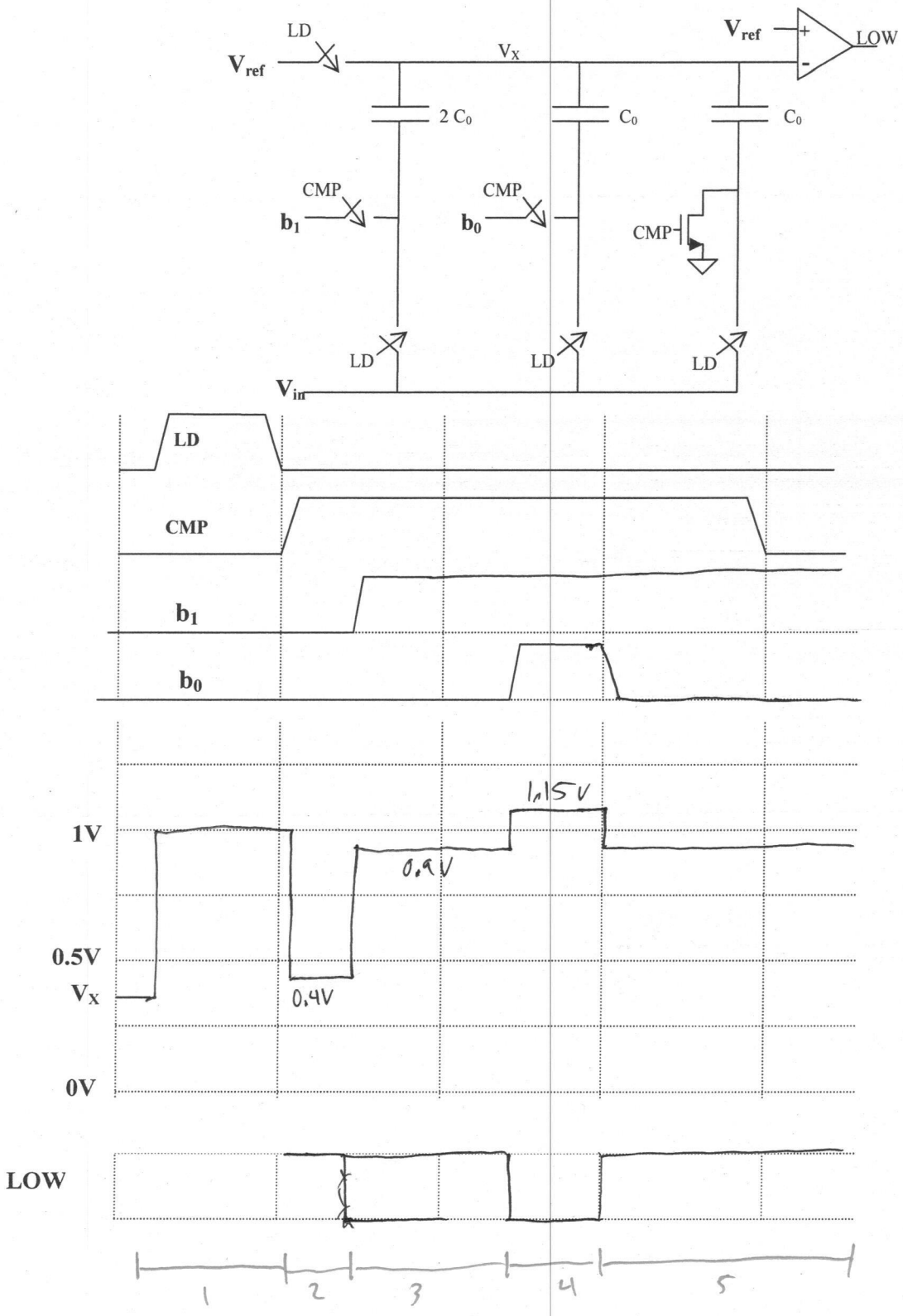
2, 6

4 maybe OK, but stability concerns

13. In the following 2 bit ADC circuit, LD and CMP are non-overlapping clocks. There is a SAR circuit which drives b1 and b0 based on LOW. Assume that the RC time constants are fast compared to the time scale below. V_{ref}=1V. b_1 and b_0 are either 0 or 1V.

a. What binary value should the SAR report when $\mathbf{V_{in}=0.6V}$? 10 2 pts

b. Assuming $\mathbf{V_{in}=0.6V}$, **carefully sketch** the waveforms on Vx and LOW, and **continue the waveforms for $\mathbf{b_1}$ and $\mathbf{b_0}$** on the graph provided below.



5 regions, 2 pts each